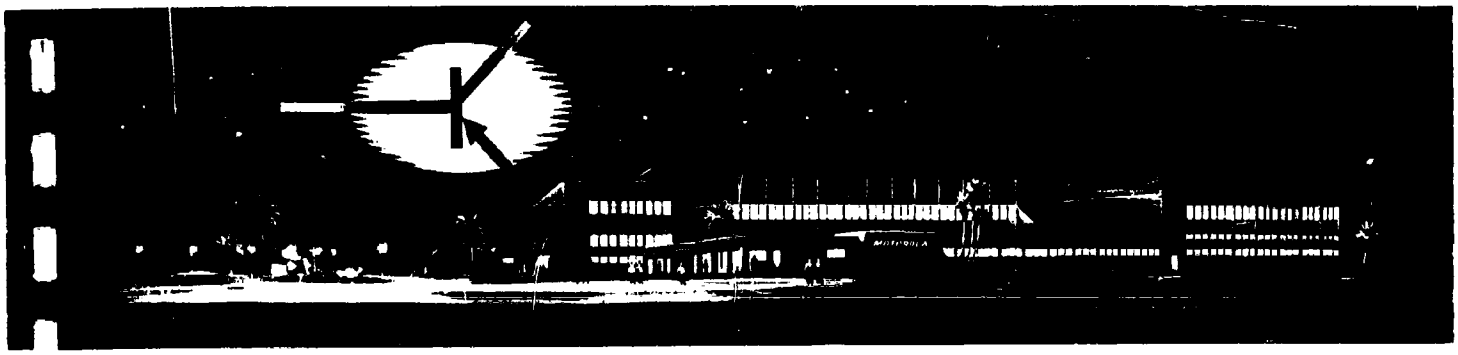
FIRST QUARTERLY REPORT
COMPATIBLE TECHNIQUES
FOR
INTEGRATED CIRCUITRY

U. S. AIR FORCE
CONTRACT NO. AF33(616)8276

prepared for

U. S. AIR FORCE
AERONAUTICAL SYSTEMS DIVISION
WRIGHT-PATTERSON AIR FORCE BASE, OHIO



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Period of 4 May 1961 - 4 August 1961

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Prepared by

MOTOROLA INC.
SEMICONDUCTOR PRODUCTS DIV.
PHOENIX, ARIZONA

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1.0 INTRODUCTION

This report covers the first quarter's efforts in developing compatible techniques for integrated circuitry on contract AF 33(616)8276.

Most of the effort to date has been spend in developing process techniques which are necessary for integrated circuit fabrication. This effort has been both in morphological areas and thin films as applied to semiconducting substrate.

Further efforts in perfecting our epitaxial techniques are reported. A program has been started to develop and fabricate typical circuits which are practical for a wide range of high and low frequency amplifier applications. This period terminates all contractual efforts in the development of logic circuitry.

2.0 PROCESS DEVELOPMENT AND PROCESS COMPATABILITY

2.1 EPITAXIAL GROWTH

2.1.1 Silicon Epitaxial Layers

The development of techniques for growing single and multilayer structures of controlled thickness and resistivity continues.

Presently, silicon films are deposited with the growth 1,1,1. oriented. Deposition is carried on in a horizontal, open tube, flow system, with the reactant bases flowing parallel to the direction of growth propagation. RF induction heating is used with a 1 ½" wide X 6" long X ¼" thick graphite susceptor which accommodates seven 3/4' diameter wafers placed in a row.

The reaction being used is the thermal decomposition of trichlorosilane which is carried by hydrogen. Several systems for pickup of the vapor and the control of its concentration in the gas phase have been investigated. These systems were essentially the same, in that metered hydrogen passes over trichlorosilane liquid, held at constant temperature, and picks up the vapor via evaporation transporting it to the reaction zone. A diagram of the system finally settled on

is shown in Figure 2-1. Concentration control with this system is well within ± 10%, allowing ± 10% film thickness control. This system also has the advantage of allowing one to vary the concentration of the vapor over a wide range.

It has been found that the rate of silicon deposition per unit area Microns/Min is nearly independent of gas flow rate and substrate temperature, but depends almost entirely on the concentration of trichlorosilane in the hydrogen carrier gas. A simple linear equation relates the deposition rate to the concentration. This is

$$D_{si} = K\, Y_{HSiCl_3} ,$$

where

D_{si} = Average deposition rate of silicon in Microns/Minute

Y_{HSiCl_3} = Mole fraction of trichlorosilane in the gas phase -- Dimensionless

K = Reaction rate constant 60 Microns/Minute

This equation indicates the reaction is a simple decomposition reaction with the deposition rate depending solely on the diffusion rate of trichlorosilane to the substrate surface, and should be proportional to its concentration in the gas phase. It has been found that the deposition rate varies from the head wafer on the susceptor to the last wafer by

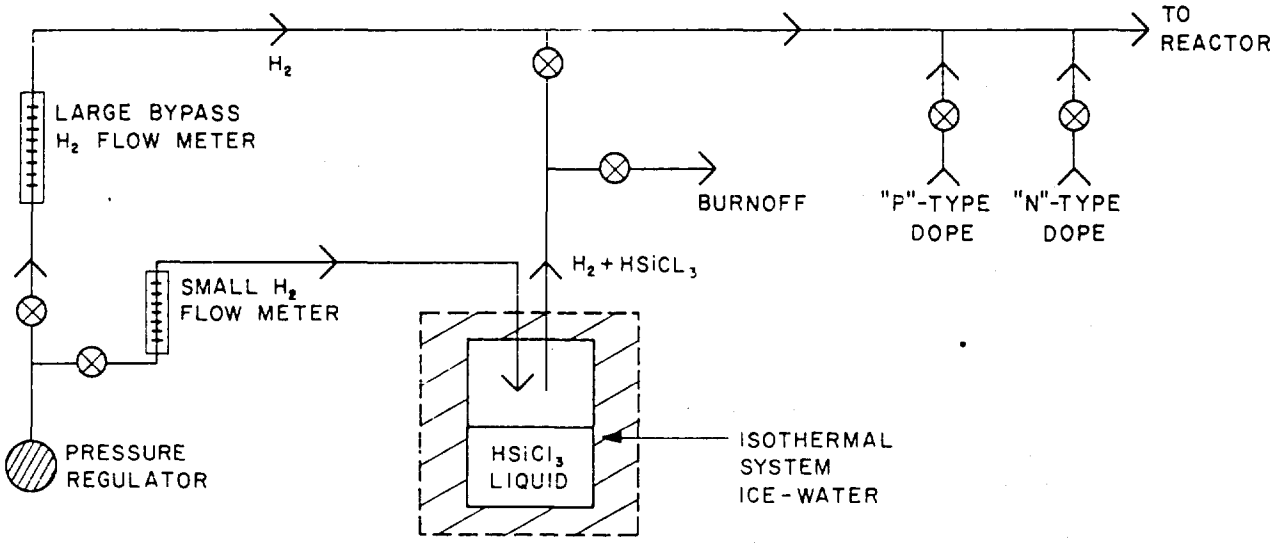


Figure 2-1. Flow Schematic for $HSiCl_3$ Pick-up

40% with the greatest growth on the head wafer. It is also possible to find growth variations across the wafers. These effects are probably due to the Prandtl boundary layer which theory indicates should be smallest at the leading edge and become thicker progressing down the susceptor. This type of layer would allow greater diffusion of trichlorosilane to the first wafer than to the last.

2.1.2 Closed Tube Epitaxial GaAs

A disproportionation reaction between GaAs and hydrogen chloride gas leads to the deposition of GaAs on a suitably prepared germanium wafer:

$$3GaAs + 6\ H\ Cl \rightleftharpoons GaAs + 2\ Ga\ Cl_3 + \tfrac{1}{2}\ As_4 + 3\ H_2$$

With the reactants at a higher temperature than the products, the reaction goes from left to right. Single crystal films are deposited with the reactants in the range of 700 - 750°C and a 40° - 70°C temperature difference between reactants and substrate.

Present surfaces are terraced and pyramided depending upon growth conditions (Figure 2-2). In order to attain smooth surfaces on the deposited films a series of runs was made. Source and substrate temperatures and time of reaction

Flat Terraced Surface of Single Crystal GaAs. 50×

Severely Pyramided Surface of Single Crystal GaAs. 50×

Figure 2-2. GaAs Crystal Surfaces

were held constant and the H Cl pressure progressively reduced. It was expected that as the pressure was lowered the reaction would be slowed and the growth rate reduced. It appears that the growth rate must be lowered in order to produce smoother surfaces.

However, as the H Cl pressure was reduced, the growth rate was found to increase (Figure 2-3). The GaAs charge and germanium wafer are separated in the ampoule by a distance of five inches. Since deposition cannot start until the reactants reach the substrate, gas diffusion down the ampoule may be controlling the growth rather than reactant pressure over the substrate. Lower presures then are believed to give a faster diffusion rate of reactants to the substrate and are producing a heavier growth in two hours.

An attempt was made to run a series of ampoules with pressure and source temperature constant, varying only substrate temperature. However proper control of pressure and temperature was not possible and results were erratic.

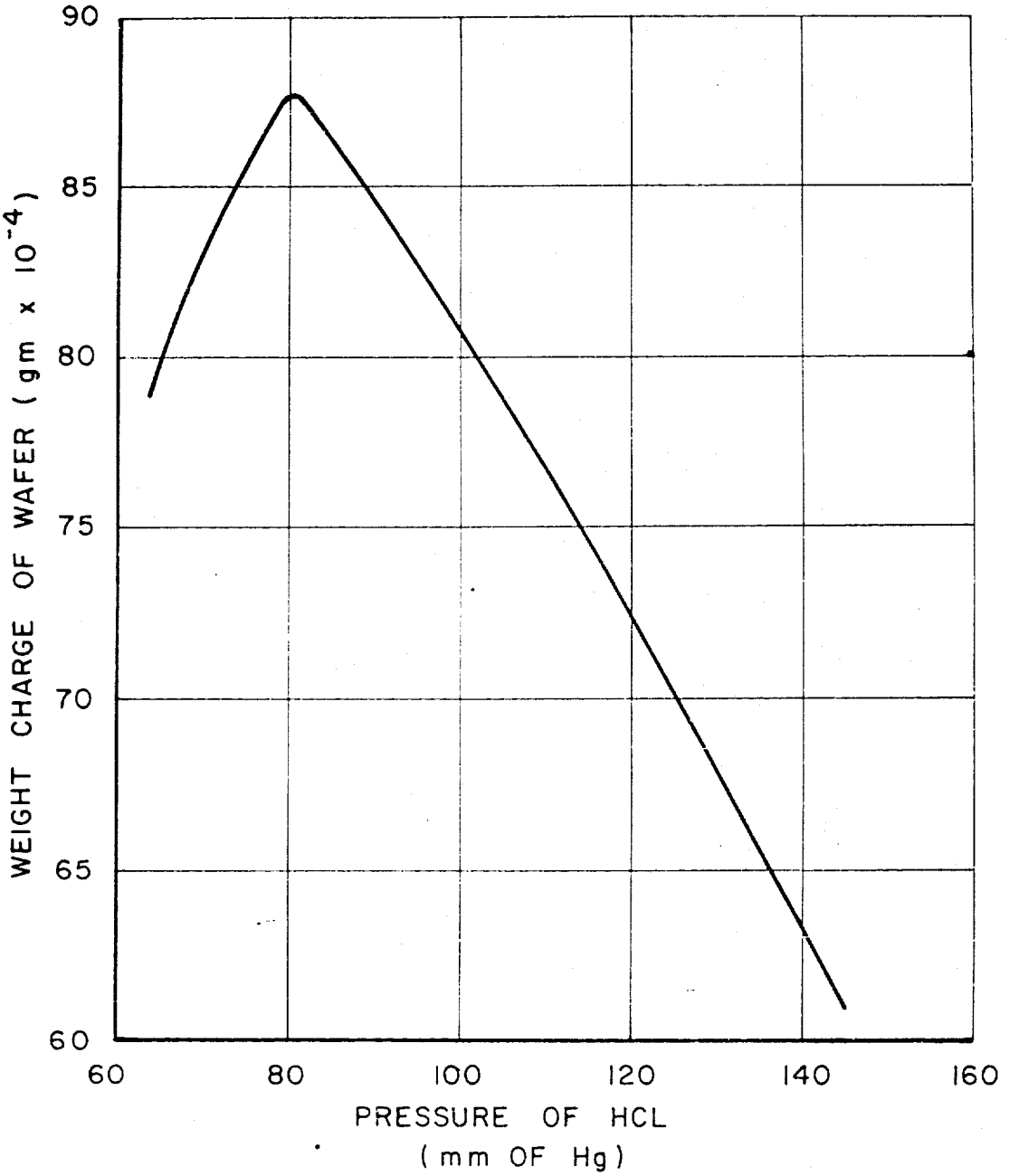


Figure 2-3. Weight Gain of Germanium Substrate as a Function of HCl Charged Pressure at 30°C During 2 Hour Growth Period. Substrate Temperature 703° ±4°C

Deposit thicknesses are measured by beveling and staining techniques. Germanium substrates used to date have been heavily doped p-type. Beveling and staining reveals an n-type diffused germanium layer beneath the GaAs. Calculations confirm that arsenic would produce junctions at the depths measured.

Thermal probe readings of the GaAs show the material to be n-type. Since there is an initial reaction between H Cl and germanium, Ge Cl_4 is also found in the gas phase and is probably doping the GaAs upon deposition.

Special Problems:

The gas measuring chamber for H Cl has been redesigned to allow more precise measurement of low H Cl pressures. This should give better control of pressure as a growth parameter. Also better control and measurement of temperatures is necessary.

The question of interdiffusion between the epitaxial GaAs and germanium substrate must be better understood as far as possible diffusion of germanium into the GaAs is concerned. The question of contamination of the GaAs by vapor phase doping of germanium must also be answered.

2.1.3 Evaluation of Epitaxial Layers

A great amount of time has been spent on the analysis of epitaxial structures. This analysis has proceeded in two general directions. The first is that of actually picturing or showing the various structures that are grown. The second is the use of an anodization technique for determining the resistivity gradient as a function of depth below the surface.

In the direction of showing the structures, methods have been developed for the delineation of various silicon epitaxial structures. Using these procedures, it has been possible to show various resistivity fluctuations within a region of one conductivity type, as well as P-N junctions. In this manner, delineated pieces may then be measured for region thickness by use of an optical interferometer.

The chemical solution that is used for delineating different silicon structures is composed of hydrofluoric acid, hydrogen peroxide, and water. The proportions vary depending on the structure.

The silicon to be delineated is beveled at an angle of 1° 30' although this angle has no effect on subsequent staining. The chemical solution is applied to the beveled surface and using a concentrated white light the structure is shown.

The actual mechanism involves a slight oxidation. The rate of oxidation is different for the different regions within the structure. The results are readily visible. Typical examples are shown in Figure 2-4.

The second direction for analysis is that of anodization. The anodizations have been carried out on P-regions only. These P-regions were grown on an n-region. Thus, four point probe measurements of sheet resistivity could be made. From this and the thickness data, secured from beveling and staining, it was possible to calculate bulk resistivity. The anodizing solution is composed of sodium tetraborate and boric acid. Several plots of resistivity versus depth were made. Two typical ones are shown in Figure 2-5.

In practice approximately one-thousand Angstroms is anodized, removed with hydrofluoric acid and the resistivity is measured. As can be seen from the graphs, the resistivity increases near the junction.

Another method of determining the properties of epitaxial layers is through the analysis of characteristics of devices that are made incorporating the epitaxial layers. For example, transistors were made with diffused emitters and bases and having epitaxial collector regions. Through a detailed

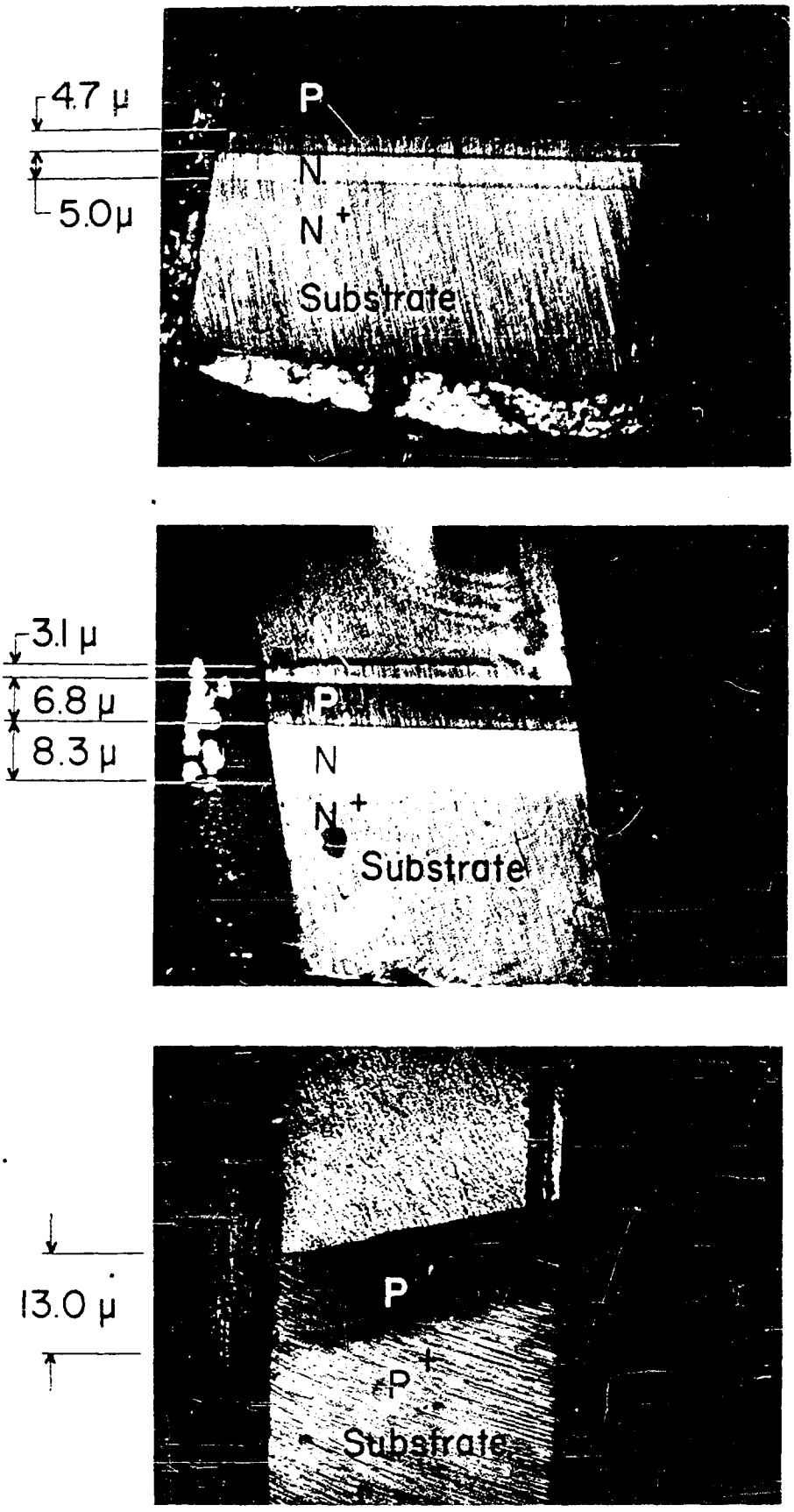


Figure 2-4. Layered Silicon Structures

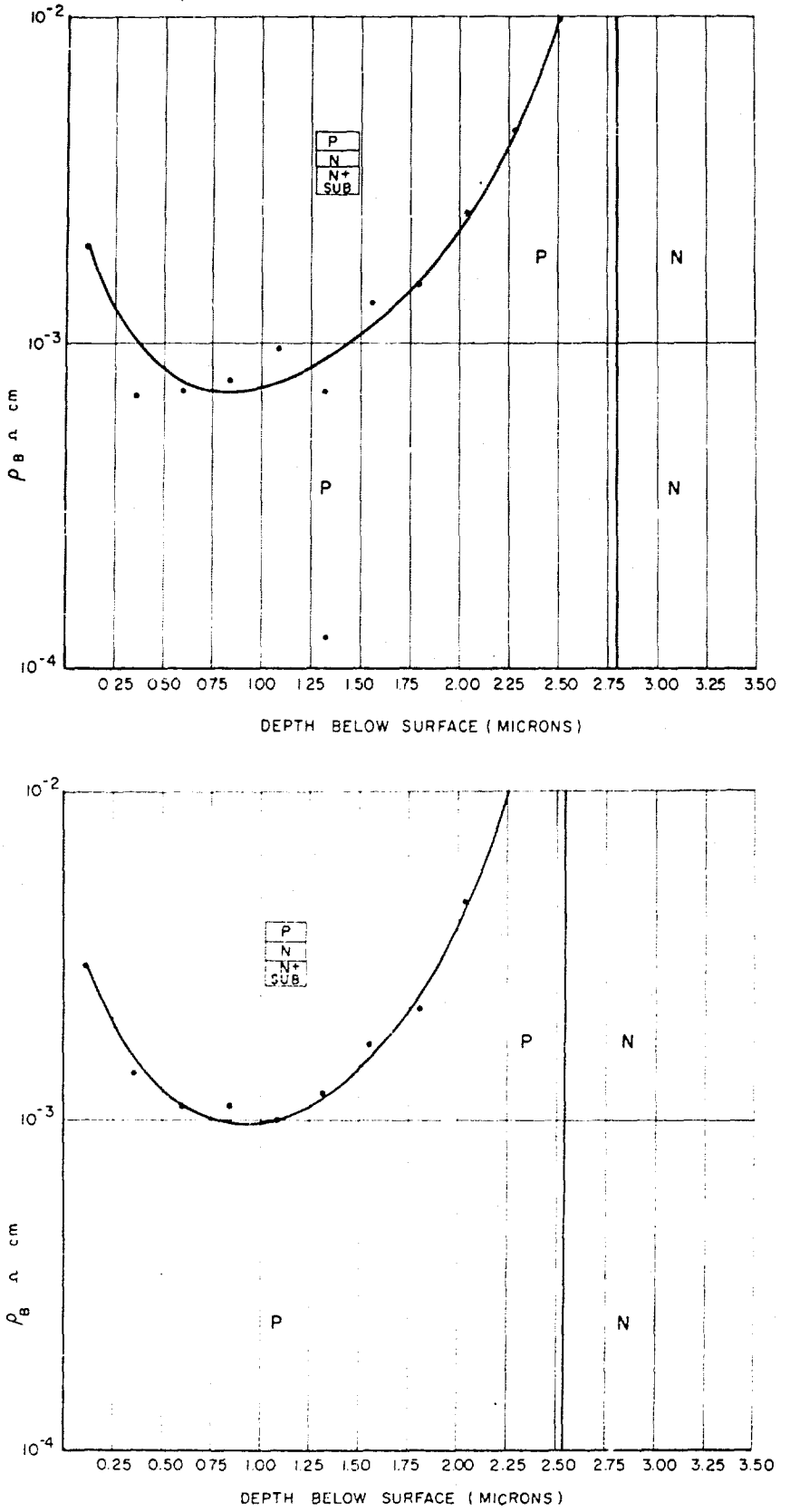


Figure 2-5. Typical Plots of Resistivity Versus Depth

analysis of their characteristics, information on the resistivity, effective thickness, and structural perfection of the epitaxial layers was obtained.

2.1.4 Evaluation of Multiple Layer Epitaxial Growth Through Active Structural Fabrication

With the advent of the techniques for growing epitaxial films of silicon and germanium, the question arises as to how the method compares to a well established technique such as diffusion. The present commercial epitaxial transistors consist of thin epitaxially grown collector regions into which the base and emitter are diffused. By controlling the impurity during growth, it is theoretically possible to produce a completely grown epitaxial structure. One must then decide what advantages, if any, accrue. Since this is exactly the problem faced by those who wish to make epitaxially grown integrated circuits, it is felt that building a 2N834 state-of-the-art transistor using epitaxial techniques is a suitable first step in building complete circuits of these films.

There are several advantages to this approach. For instance, a standard for comparison is readily available in the 2N834, commercially available, transistor with which

considerable experience has already been accumulated. This standard has the same geometry so we can compare grown junctions with diffused junctions both highly doped and lowly doped (emitter to base and base to collector junctions respectively). We can also compare these transistors with non-epitaxial units such as the 2N706.

Several hundred units have been made that fulfill the essential 2N834 specifications. These have grown base and collector regions and diffused emitters. A considerable amount has been learned about the material requirements for making such units. For instance, units have been successfully made with emitter base junction depths that range from 0.4 to 2.4 microns. Base widths vary from 0.2 to 1.3 microns. The total emitter and base region thicknesses have varied from 1.4 to 3.3 microns. The base region resistivities on successful units have ranged from 0.7 to 0.04 ohm-centimeters. The present material specification for making the grown base and collector unit are as follows:

1) polished n-type substrate 5 ± .5 mils thick of .01 ohm-cm resistivity;

2) epitaxial n-type film 6 microns thick of 2 - 5 ohm-cm resistivity;

3) finally a p-type film on top having a thickness of 1 to 2 microns; a resistivity ρ_b such that

$.05 < \rho b < .1$ ohm-centimeter. Such material can be supplied to specification now that the effects of the various processing steps on the material have been determined.

As an illustration, the impurity doping profile has been reproduced for a typical unit in Figure 2-6. The first thing to note is the profile labeled 1 which is the ideal structure which the crystal grower tries to grow, with step junctions separating flat regions of constant doping.

Curves labeled 2 (dashed curves) are those which exist at the end of the film growth period when the wafers are ready to be used for making devices. Note that the step junctions no longer exist but in their places are diffused type gradients. These have arisen from the diffusion of impurities from regions of high concentration to regions of lower concentrations.

The curves labeled 3 are the final doping profile of the device after growing a masking oxide, diffusing in the emitter, and alloying.

Note that in order to come out with an actual base-collector junction depth of 2 microns and a high resistivity n collector region 6 microns thick the grower must actually grow 12 microns of film of which 10.9 microns is n-type and

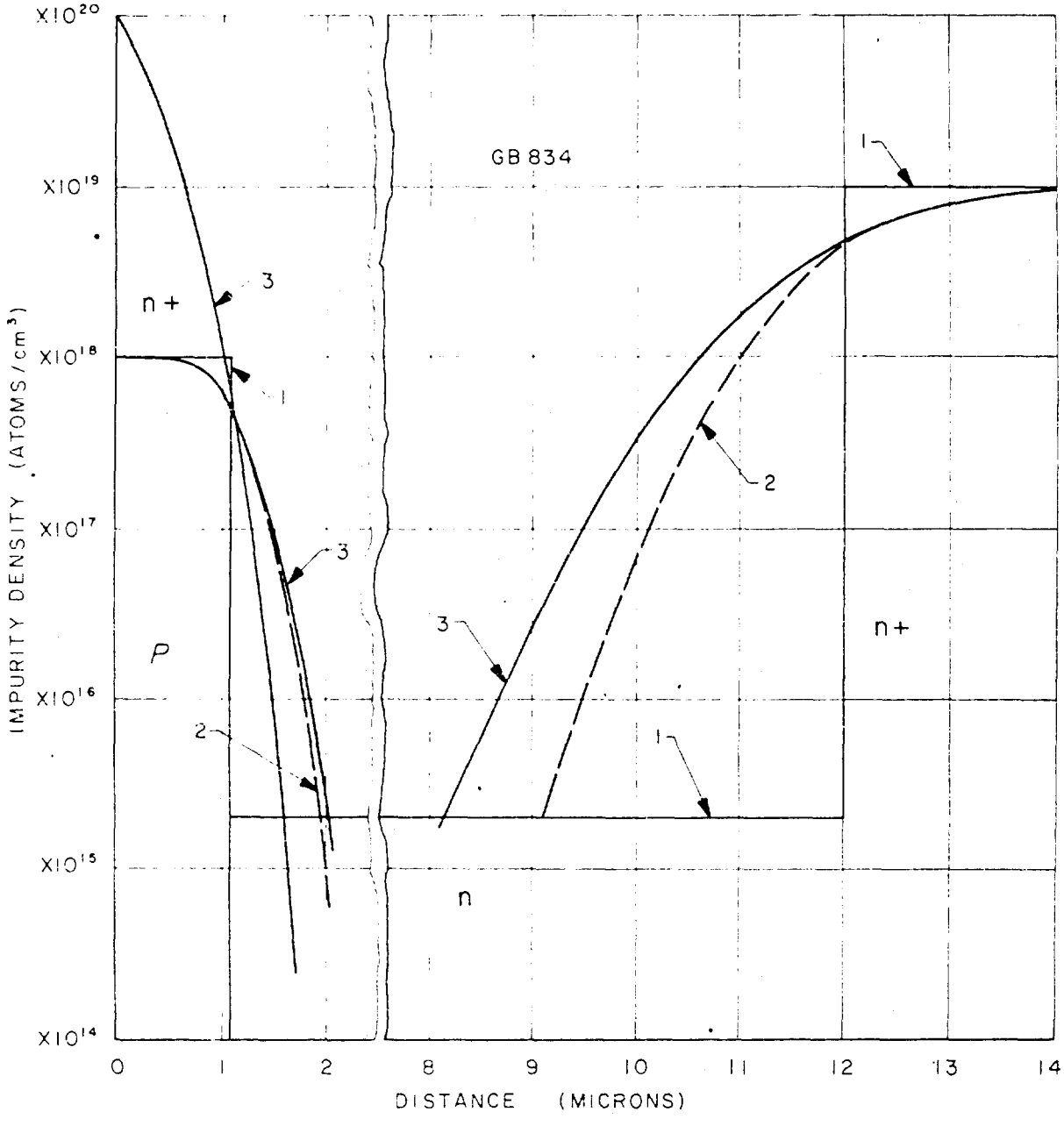


Figure 2-6. Impurity Doping Profile in Grown Base Silicon Transistor

1.1 micron is p-type. Diffusion that occurs during growth then gives the desired dimensions.

3.0 COMPATIBLE THIN-FILM TECHNOLOGY

3.1 INTRODUCTION

During recent years the technology of thin films has been extended to serve as a new method for manufacturing electronic components and systems. In general, passive substrates such as glass or ceramic have served as mechanical supporting members for the thin-film circuits. The thin-film deposition processes which have been developed, are those which are compatible with glass or refractory ceramic substrates. This portion of the report discusses the programs and progress made to date on the development of thin-film technologies which are compatible with semiconductor substrates. The aim is to provide low cost processes for constructing thin-film electronic components on small areas of semiconductor substrates without destroying active elements previously constructed within the substrates.

The following thin-film programs have been initiated on this contract to establish compatible processes for constructing thin-film components on semiconductor substrates.

In general, they are extensions of programs which previously have been sponsored entirely by Motorola.

3.2 DEPOSITION OF GLASS FILMS

This task has been initiated to develop means for depositing glass films on semiconductor substrates by means which are compatible with other thin-film and semiconductor materials and technologies. Techniques previously developed at Motorola for depositing glass films are to be refined for this particular application. The goals are to provide glass films for use as:

a. A dielectric film for capacitors

b. An electrical insulating film for conductor cross-over insulation

c. An encapsulant film for thin-film components.

3.2.1 Pyrolysis

Pyrolysis is a general method for forming thin films, both inorganic and organic. By the application of heat, a volatile chemical compound is decomposed into an element or a simpler compound which is non-volatile, plus various volatile byproducts. For example, tri-isopropyl aluminate is pyrolyzed to alumina as follows:

$$2Al(OC_3H_7)_3 \xrightarrow[800\text{-}1000\,^\circ C]{\Delta} Al_2O_3 + 3C_3H_7OH$$

The alumina deposits on a substrate as a thin film of refractory, insulating material, while the byproducts pass out of the deposition zone and are discarded.

Pyrolysis is distinguished from vapor plating in that it comprises thermal decomposition of a vapor in an inert carrier gas such as nitrogen or argon, whereas vapor plating involves the reaction of a vapor with an active carrier gas.

In the usual pyrolysis technique, a substrate is placed in a controlled heat furnace (see Figure 3.1). Carrier gas of known pressure is metered so that some of it passes through the volatile starting material, which may or may not be heated. The carrier gas thus brings a controlled amount of starting material vapor into the furnace. Pyrolysis occurs, and the desired product is deposited on the substrate. Furnace temperatures from 180° to 1500°C are normal, and pressures from atmospheric to as low as 2 mm/Hg are used. It can be seen that the technique is inefficient, since more product is usually deposited on the furnace walls than on the substrate. This can be overcome, however, by employing

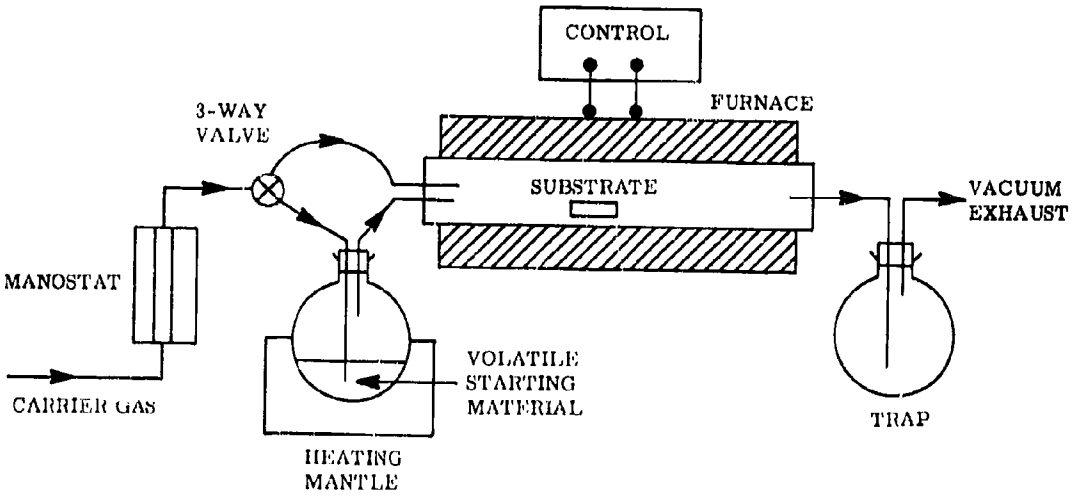


Figure 3-1. Basic Pyrolysis Equipment

induction heating on a conductive block which also serves as substrate support.

Volatile byproducts of the pyrolysis are exhausted to a trap by the application of a slight differential pressure.

One of the requirements of engineering a thin film onto an integrated circuit is that the substrate time-temperature product during deposition should not be such as to permanently change electrical and physical characteristics of a set of circuit elements already fabricated thereupon. In this connection, Motorola has done extensive work on a process for depositing pure silica, silica based glasses, or silicone polymers on substrates the temperature of which does not exceed 200°C. This approach utilizes a Motorola innovation called double-zone pyrolysis.

Figure 3.2 schematically shows an apparatus for double-zone pyrolysis. The essential feature is separation between the pyrolysis and deposition zones, so that the latter can be held at a much lower temperature than the former. Thus, by passing a mixture of silicon and boron containing organic compounds through the pyrolysis zone at 800-1000°C, a clear borosilicate glass can be deposited on a substrate whose temperature need not rise above 150°C. Because it is

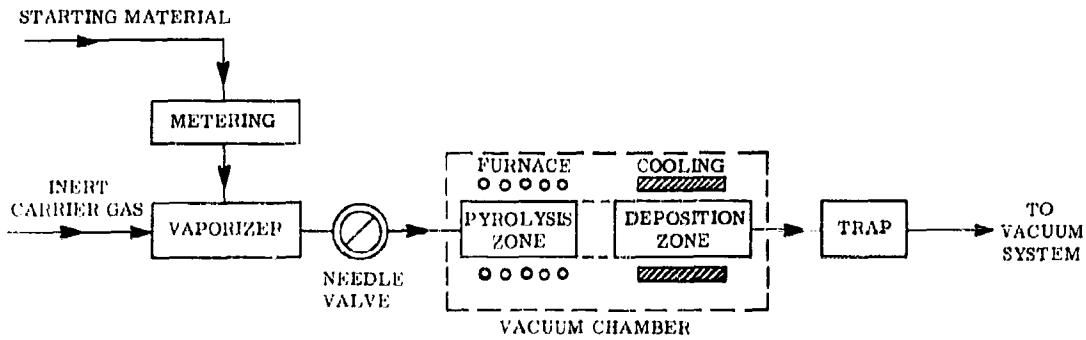


Figure 3-2. Double-Zone Pyrolysis Equipment

necessary to ensure that organic byproducts of the pyrolysis do not condense with the glass on the cooler substrate, it is necessary to maintain both zones at reduced pressure (3-5mm/Hg). Furthermore, when producing pure silica glass deposits, care must be used to exclude moisture as a byproduct of the pyrolysis, since pure silica has high affinity for water molecules.

The pyrolytic application of inorganic glasses offers a number of advantages. These include:

1. Freedom from grains and pinholes; ability to fill in irregularities and "go around corners."
2. Low deposition temperature compatible with other materials and processes.
3. Excellent electrical properties (high dielectric strength, low loss, etc).
4. High chemical and physical durability.
5. Low volume permeability to moisture and a low permeability along the interface between the glass and a dissimilar material.

3.2.2 Technical Effort for the Reported Period

Effort was devoted during this report period to the investigation of means to increase the Q of glass capacitors for applications at high frequency. The series resistance introduced by the sheet resistance of the thin-film metal

electrodes has been identified as the major source of loss for these capacitors. The effect of various metal films utilized for the electrodes was studied as was the aging characteristics of capacitors constructed with aluminum electrodes. The source material utilized in the double-zone pyrolysis glass deposition equipment to form the quartz dielectric films was dibenzyl-diethyl-orthosilicate.

Table 3.2.1 presents data obtained in the study of the variation of dissipation factor and capacitance with frequency for various electrodes. It is important to note from Table 3.2.1 that in all capacitors except those constructed with platinum electrodes, the dissipation factor decreased with increasing frequency. This is attributed to the effect of electrical leakage of the dielectric material where its effective parallel resistance is such as to compete with the capacitive reactance of the device at lower frequencies. The decrease in capacitance with increase in frequency could be attributed to interfacial polarization brought about by a possible modification of the crystal layers of the dielectric.

Early in the investigation it was believed that the interfacial layer between the electrode material and the

TABLE 3.2.1

Sample#	Electrode Material	Frequency	C pf	D.F.%
1.	Platinum	1 KC	893	4.0
		10 KC	856	2.8
		100 KC	837	4.3
2.	Platinum	1 KC	978	3.7
		10 KC	945	2.3
		100 KC	923	3.1
3.	Aluminum	1 KC	837	4.8
		10 KC	808	2.1
		100 KC	788	1.9
4.	Aluminum	1 KC	654	4.2
		10 KC	632	2.0
		100 KC	619	1.8
5.	Aluminum	1 KC	717	4.5
		10 KC	692	2.5
		100 KC	625	1.8
6.	Gold	1 KC	750	4.0
		10 KC	735	3.0
		100 KC	715	2.5
7.	Tin-Gold	1 KC	813	3.0
		10 KC	790	2.1
		100 KC	778	0.9
		500 KC	775	0.0

dielectric contributed heavily to the loss factor. A series of capacitors constructed with a variety of electrode materials were investigated. It was determined, however, that the resultant dissipation factor as measured at 50 megacycles per second correlated directly with the sheet resistance of the electrode material. The problem resolves itself then to the deposition of stable electrodes to low ohm-per-square values. To date typical results obtained for small valued glass dielectric capacitors at 50 mc is presented in Table 3.2.2.

The RC product of unencapsulated capacitors constructed with pyrolytic glass films is in the order of 10 ohm farads. It is expected that encapsulation will reduce surface leakage currents and further increase this product.

3.3 TANTALUM OXIDE CAPACITORS

Tantalum oxide non-electrolytic thin-film capacitors are attractive for use with integrated circuits because of the relatively large value of capacitance which they provide per unit area. Tantalum oxide thin-film capacitors have been developed to a high degree for use on passive substrates by Motorola. They provide a capacitance voltage product of 5

TABLE 3.2.2.

Electrode Material	C, pf	D.F., %@50MC
Sn-Au alloy	5.8	12.5
Sn-Cu alloy	20	5.0
Cu	13	5.9
Ag	23	5.2

microfarad volts per square centimeter of substrate area for a single dielectric layer capacitor.

The purpose of this task is to modify our present techniques to enable the construction of such capacitors on semiconductor substrates. The problem areas are:

a. Develop means for depositing adherent tantalum films on semiconducting substrates.

b. Determine methods for attaching electrodes to the tantalum film to enable anodization of the film in an electrolytic bath.

c. Deposition of counterelectrodes.

d. Control of dissipation factor at high frequencies.

e. Electrical and aging tests.

Motorola has developed a highly successful technique for the fabrication of precise and voltage stable thin-film tantalum capacitors. An advance in the art was made when the Motorola team developed a method of depositing ultra pure tantalum metal films on glass and ceramic surfaces by vacuum evaporation. Subsequent controlled anodization and the deposition of counterelectrodes produce capacitors which exhibit the following characteristics:

1. Capacitance variation versus temperature (-55°C to 150°C) is less than 5 per cent.

2. D.C. leakage currents of less than .060 microamperes at 25 vdc, 125°C for 0.01 uf capacitors.

3. Average D.C. leakage at room temperature at 25 vdc of less than .001 microamperes for 0.01 uf capacitors.

4. Dissipation factors at 1 kc in the range of 0.7 to 1.5 per cent over the temperature of -55°C to 125°C.

5. Rating of 5 volt microfarads per square centimeter at 50 per cent of breakdown voltages.

The vacuum deposition technique utilizes an electron beam evaporator and a water cooled anode crucible. This technique coupled with proper substrate cleaning methods plus the use of a heated substrate make it possible to obtain well adhering, uniform tantalum films of high purity measuring approximately 3000 Å thick. The film is then masked to prevent oxide growth over tantalum areas where electrical connections are to be made. The films are then anodized in an electrolytic bath by maintaining the current density at a fixed low level until the desired forming voltage is reached when the current is then permitted to drop to zero. The thickness of the resulting layer is directly proportional to the anodizing voltage. The counterelectrode is then evaporated over the anodized film, leaving a few

thousandths of anodized layer exposed to provide adequate insulation along the capacitor edges. Capacitors can be made to tolerances of ±5 per cent in the 0.01 microfarad range using these methods.

3.3.1 Accomplishments for the Reported Period

Effort was devoted during this report period to the improvement of yield of tantalum film capacitors and to the reduction of the dissipation factors at elevated frequencies.

Modifications were made in the electron beam tantalum evaporation equipment which greatly improved the yield of acceptable capacitors. The modifications were those which provided for a cleaner vacuum system and a resultant reduction in the contamination of the deposited tantalum film. The use of stainless steel masks for delineating the geometry of the tantalum film appeared to further improve the capacitor yield over that experienced with beryllium copper masks. This change was recommended in that high vapor pressure copper oxide which could form on the old mask was suspected as a source of contamination of the tantalum film. This in turn would be a source of contamination of the dielectric film which is formed by subsequent anodization of the tantalum.

A major effort of this period was devoted to the improvement of dissipation factor for tantalum capacitors at high frequencies. As with the glass film capacitors discussed previously, the major source of loss is attributed to the sheet resistance of the thin-film electrodes. A major limitation to improving the conductivity of the tantalum electrode has been the experienced mechanical stripping of thick tantalum films from the substrate during anodization. Films deposited to a maximum thickness of 3000 Angstrom units adhere well to the substrate while those which are appreciably thicker strip during the anodization process. The thickness and the resulting sheet conductivity of the tantalum electrode decrease during the anodizing process when the outside surface of the tantalum conducting film is converted to the insulating oxide. In order to obtain low sheet resistance tantalum electrodes, a thick layer of aluminum is deposited onto the substrate prior to the deposition of the tantalum film.

The counterelectrode is constructed of gold which is bonded to the oxide material by an extremely thin film of chromium (deposited from nichrome alloy). A series of capacitors constructed by this manner was manufactured during this period with acceptable yields. The value of the

capacitors was 2000 uuf and they were constructed for 50 volt operation. The leakage current at 10 volts (Ta-t) varied between 1.2×10^{-10} and 2.4×10^{-12} amperes. The dissipation factors measured at 1 kc varied between 0.06 and 0.3%. This compares with standard tantalum capacitors which exhibit room temperature dissipation factors of 0.78 to 0.98 per cent at 1 kc.

Aging evaluations and tests at elevated frequencies will be made during the next report period.

3.4 TIN OXIDE RESISTOR FILMS DEPOSITED ON SEMICONDUCTOR SUBSTRATES

In order to provide thin-film resistors of high value which occupy a small substrate area, it is required that resistor films possessing large ohm-per-square values be developed. Metals and their alloys, due to their excellent conductivity, are limited to providing manufacturable and reproducible resistive films of 300 ohms per square maximum. The semiconducting materials must be resorted to in order to provide larger ohm-per-square values. This laboratory has in the past developed a tin oxide semiconducting film for use on glass and refractory ceramic substrates which possesses a sheet resistance of 5,000 ohms per square. The deposition

temperature and the fact that Group III and V elements are also utilized as minor constituents in the film, indicate that in order to be compatible with semiconducting substrates, a low temperature deposition process must be developed. The effort of this program is to be directed along lines currently under development at Motorola for constructing metal oxide films at low temperature. The goals of this program are:

a. Develop a low substrate temperature process for depositing pure tin oxide films.

b. Develop means for doping the tin oxide films with Group III or Group V elements.

c. Develop masking and etching methods for delineating the geometry of the resistive films which are compatible with the semiconducting substrates.

3.4.1 Current Work

Exploratory work was carried out during this period on the deposition of tin oxide resistive films by the low temperature decomposition of tin organic compounds. Deposition was accomplished by painting the pure compound or a solution of the compound in various solvents onto a substrate. Upon heating, the compound decomposed to form what was considered to be tin oxide.

Several tin organic compounds were studied as initial compounds from which tin oxide could be formed. The most successful film form studied produced films which varied between 8 K and 28 K ohms per square. The deposition took place at room temperature. The films, however, were physically unstable to heat in that they cracked and tended to strip from glass substrates when heated to 100°C. Films formed in a similar manner but doped with a Group V element exhibited improved physical characteristics and did not crack when exposed to 100°C temperatures.

The conclusions of this qualitative study are that forming of quality SnO_2 resistors films is doubtful by this method. The apparent shortcomings of this technique are the lack of control over the composition and nature of the organo-tin compounds and lack of control over the reproducibility of the film forming technique. During the next reporting period attention will be focused on the more appealing vapor phase low temperature deposition of tin oxide resistive films.

4.0 SEMICONDUCTOR TECHNOLOGY

The success of any large-scale integrated circuits program is contingent upon the development of fully passivated active semiconductor devices which can be interconnected in a variety of ways to form complete networks within and upon the semiconductor material. The fact that the devices are passivated or protected at their surfaces from the ambient atmosphere is beneficial in two ways; first, long-term stability and reliability of the integrated circuits is assured, providing it is operated within its electrical ratings. This is true even if the encapsulation for the network develops flaws, since the thin but impervious membrane covering the semiconductor surface is integral with the surface in the crystalline sense. Its continuity is interrupted only in non-critical areas to provide ohmic contacts. Second, great design freedom is afforded the circuit designer, for he no longer needs separate chips of semiconductor material for each circuit element which must be interconnected after the diffusion and metallizing steps. With passivated structures, many desired combinations of active and passive devices can be fabricated on a single substrate with interconnections being formed during the above mentioned steps.

Only the minimum number of necessary connections are brought out of the encapsulant, such as those which are needed to supply power to the module and input-output connections to attach to subsequent and succeeding parts of the overall system.

Considerable effort is being devoted to the development of these techniques. Early successes have included passivated planar transistors and diodes fabricated on silicon epitaxial material. Figure 4-1 shows a condensed process flowchart for silicon transistors. In the case of a planar transistor, the passivation consists of thin silicon dioxide surface layers formed at three different points in the process. The first layer is grown after growth of the epitaxial high-resistivity film of silicon upon the low-resistivity substrate. This layer is then removed by etch-reduction in local regions where diffusion of an impurity is desired; the base impurity is then diffused into these regions, being masked everywhere else by the oxide coating. The diffusion is carried out in an oxidizing atmosphere to regrow an oxide in the etch-reduced regions, making the entire surface again passivated. The oxide is again etch-reduced in local areas within the base-diffused regions, in

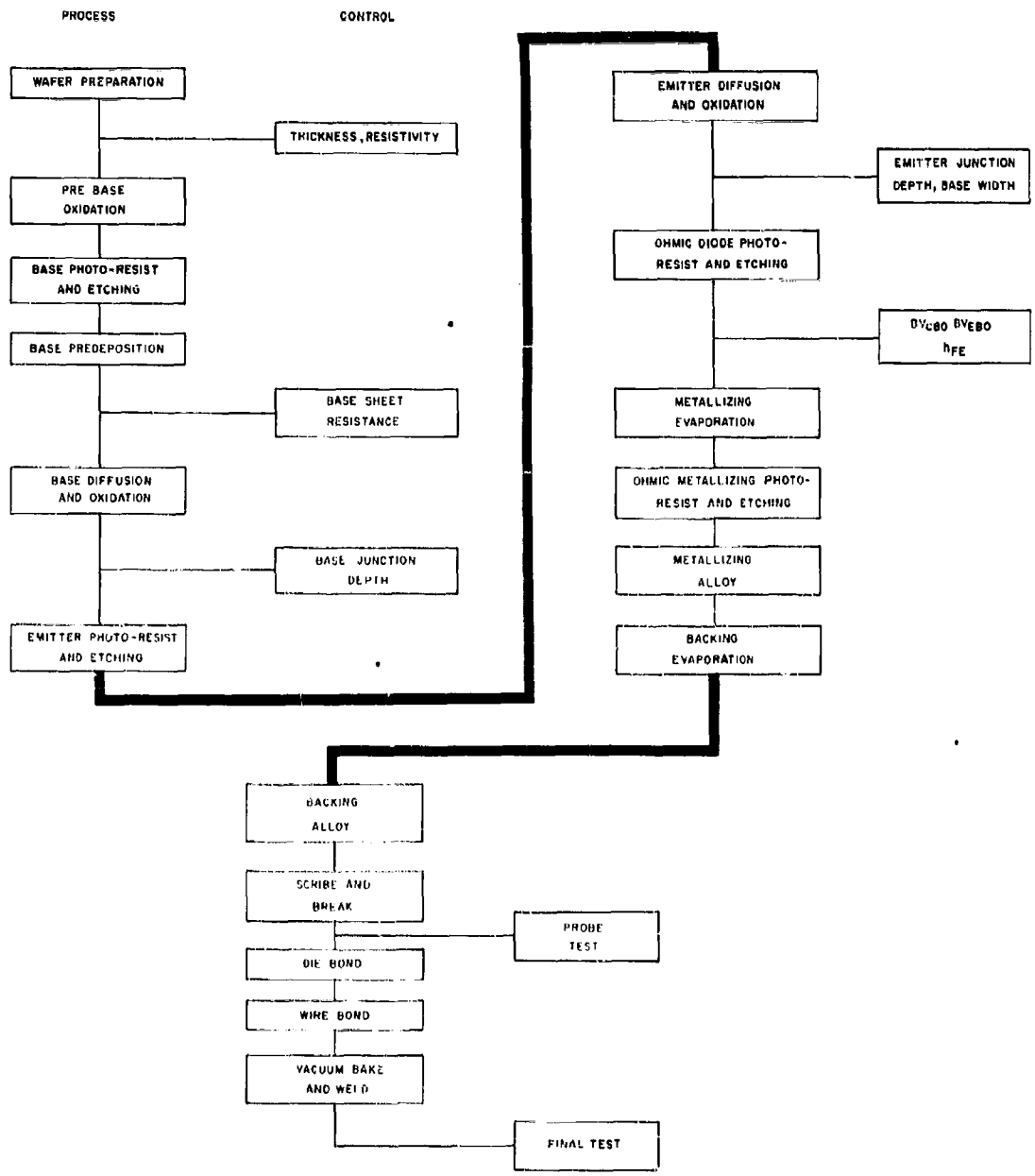


Figure 4-1. Planar Epitaxial Flow Chart

an oxidizing atmosphere. Finally, after emitter diffusion, the surface is again etch-reduced in local regions to allow alloying of metallic ohmic contact areas. This in no way disturbs the passivating qualities of the oxide since the p-n junctions in the semiconductor material are still covered with the oxide.

Devices fabricated in this manner are characterized by extremely low reverse leakage currents and high current gain at low collector current. Devices with leakage currents of 10^{-10} ampere at 50% of breakdown voltage and normalized common-emitter current gain of 0.3 at a collector current of 1 microampere are common.

Work in this area is continuing with two major objectives. First, further fundamental understanding of passivated surfaces is required, because complete integrity of the passivation is not always achieved. Further process refinements will eliminate most of the gross mechanical defects. Better understanding of silicon-silicon oxide interfaces will probably suggest suitable process changes to insure maximum protection against the environment, and provide long-term operating stability characterized by very low failure rates. Second, more complicated and useful morphologies are being

designed and built employing these techniques. Work is progressing towards the formation of several active and passive devices in a common substrate, and the intervening passivated surface areas will be employed to form interconnections which can be in the form of either simple contacts or passive networks.

Various sequences of epitaxial layer growth and masked diffusion are being pursued to obtain further information concerning the compatibility of these two techniques. For example, masked diffusion cycles are being performed before, after, and between epitaxial cycles. Results of these studies are expected to indicate how complex an integrated structure can be made using diffusion and epitaxial cycles in any desired sequence.

5.0 PHOTOMECHANICAL TECHNOLOGY

A Photographic Facility was designed to include the four basic steps necessary to fabricate photographic masks. See Figure 5-1.

The First Step (Drafting Equipment) prepares an image of the geometry to be used at a magnification which permits a tolerance variation compatible with the final mask tolerance.

This image is then reduced at the Second Step (Large Reduction Camera) to a size which is still larger than the final mask. Since this camera has a reduction capability of 40:1, most masks can be reduced in one simple reduction, thus eliminating repeated processing which is detrimental to certain aspects of image definition.

The Third Step was included in this facility for reasons of device manufacturing economy. The reduced image from the Second Station is photomultiplied by means of an accurate photo-contact-repeat mechanism until the required number of images have been deposited on a photographic emulsion.

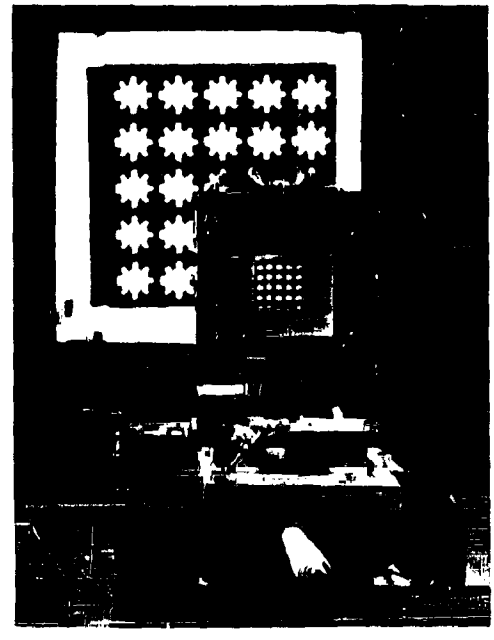
The Fourth Step is used to reduce the multiple image to its final size through a high resolving power objective.

A considerable amount of time has been spent in the alignment and calibration of the photographic apparatus described

Step 1

Step 2

Step 3



Step 4

Figure 5-1. Basic Steps of Photographic Mask Fabrication

above. The next objective is currently being pursued in optimising known photographic processes and to improve photographic techniques.

Currently, the facility supplies the necessary masks for testing various design approaches of promising geometries for experimental and integrated circuit use. Masks for multi-component circuits are in the early stages of fabrication. These masks will be used for ceramic-insulated multi-lead header integrated circuits.

The facility is continually improving on its equipment and personnel competence in order to supply the more complex masks for integrated circuit work.

6.0 ADVANCED MECHANICAL TECHNOLOGY

A Universal Integrated Circuit Wire Bonder was obtained for wire bonding (attaching minute wires to the metallized areas on the die) to extremely complicated patterns over great distances. In some extreme cases a wire as small as .0004 inch in diameter, must be attached from one area to another which is as much as one-half inch away. To emphasize the difficulty of this, it is analogous to holding one end of a 5/16 inch diameter rod 100 yards long and trying to place the other end within a one-half inch diameter area. The integrity of these bonds is such that they are undisturbed during 37,000 G. centrifuge tests of the devices. A detailed description of the bonding machine (see figure 6-1) and its purposes follows:

1. To make ohmic contact with a wire varying in size from .0004" to .002" to a metallized area on an integrated circuit as small as .0005" diameter as shown in figure 6-2. The wire is then bonded to some other part of the integrated circuit or to the ceramic substrate. This machine will accept any

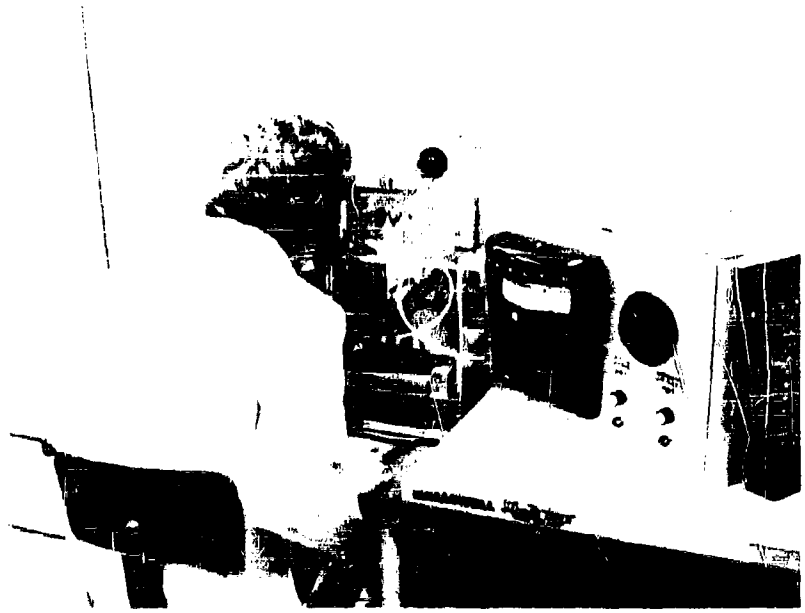


Figure 6-1. Thermo-Compression Wire Bonding Equipment

Figure 6-2. Epitaxial Star Planar Configuration

of the standard header packages such as the TO-17, TO-18, TO-5, 102, etc., as well as separate flat ceramic substrates.

2. To make ohmic contact from a die mounted on a ceramic disk to a metallized area on the disk. The present maximum distance of the separated areas is one-half inch. See figure 6-3.

3. To wire bond to any location on a .7" diameter silicon wafer and then leave the wires extended for later contacts such as shown. These wires may vary in length to a maximum of one-half inch. See figure 6-4.

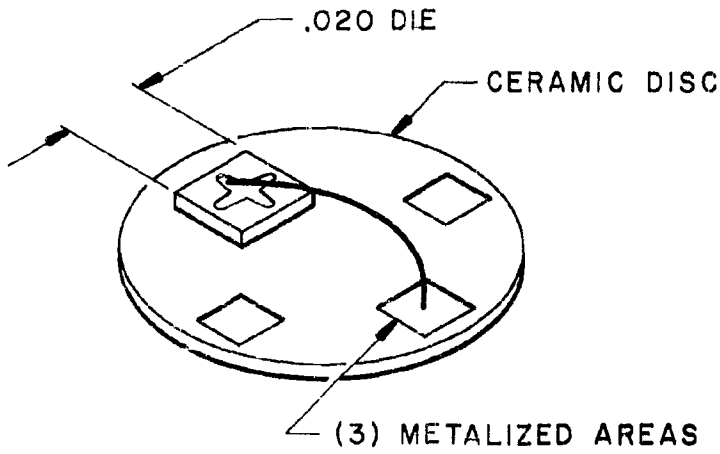


Figure 6-3. Die Interconnection

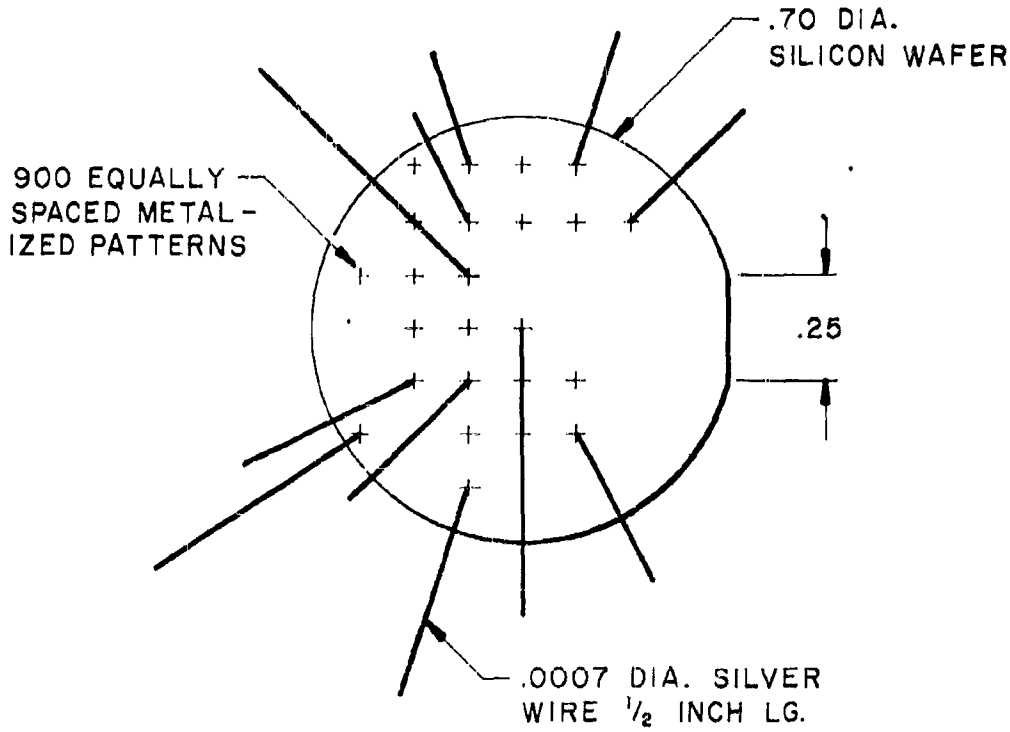


Figure 6-4. Wire Bonding on 0.7" Silicon Wafer

7.0 CERAMIC AND MODULE TECHNOLOGY

Adding the use of ceramics to the existing semiconductor technology requires the application of techniques for forming ceramic metal interfaces and metal semiconductor interfaces.

Alumina and beryllia ceramics, metallized by the "moly manganese" technique and then coated with a layer of nickel, have been produced. A photo resist applied and the metalizing is selectively removed to tolerance as close as .002 inch, depending upon the metallizing thickness. Alternatively, processes are available to apply the metallizing selectively in the desired areas. Equipment is currently being installed to selectively apply the metallizing as well as to uniformly coat the ceramics.

The semiconductor dice are bonded to the metallized areas using gold brazing alloys. The hydrophobic properties of the ceramic localize the brazing alloy to the desired areas which are metallized.

Techniques for metallizing are being investigated to obtain optimum dimensional control as well as good thermal interfaces and mechanical bonding strength. Sophisticated techniques are being developed to simplify the application of integrated circuit elements intricate arrays.

The semiconductor (and other) elements, complete with any necessary interconnecting wires, are bonded to the ceramic disk. Metallized regions around the periphery of the ceramic serve as the contacts for input, output, and power supply connections to the entire electronic configuration mounted on the ceramic. As a test vehicle, an eight-pin TO-5 header is being used. The header is gold plated. The ceramic disk and its completely inter-connected circuit is bonded to the header and then wires are attached between the peripheral metallized regions on the ceramic and the header posts. Eventually other packaging considerations will be evolved. However, at the present time, this approach requires the development of all the necessary ceramic-semiconductor technology that will be necessary in future packages, and also enables testing of state-of-the-art integrated circuits and combinations of integrated circuits through the use of known hermetic package technology.

The dimensions of the ceramic disk are (a) thickness - .020" and (b) diameter - .140".

The ceramic disk is designed to (a) provide electrical insulation from the header and between active elements when required, (b) provide a thermal conductor from the active semiconductor elements to the case, (c) provide a surface

suitable for alloying or otherwise attaching semiconductor elements and for thermo-compression bonding fine wires, and (d) provide a suitable platform, when selectively metallized, to act as the finished mounting facility for the active semiconductor elements.

One selective metallization pattern is shown in figure 7-1. A maximum of seven active semiconductor elements may be mounted and interconnected on this disk. The eight metallized areas on the perimeter of the disk correspond to the location of the eight pins in the header.

The connecting wire may either be bonded directly from element to post or from element to metallized area to post.

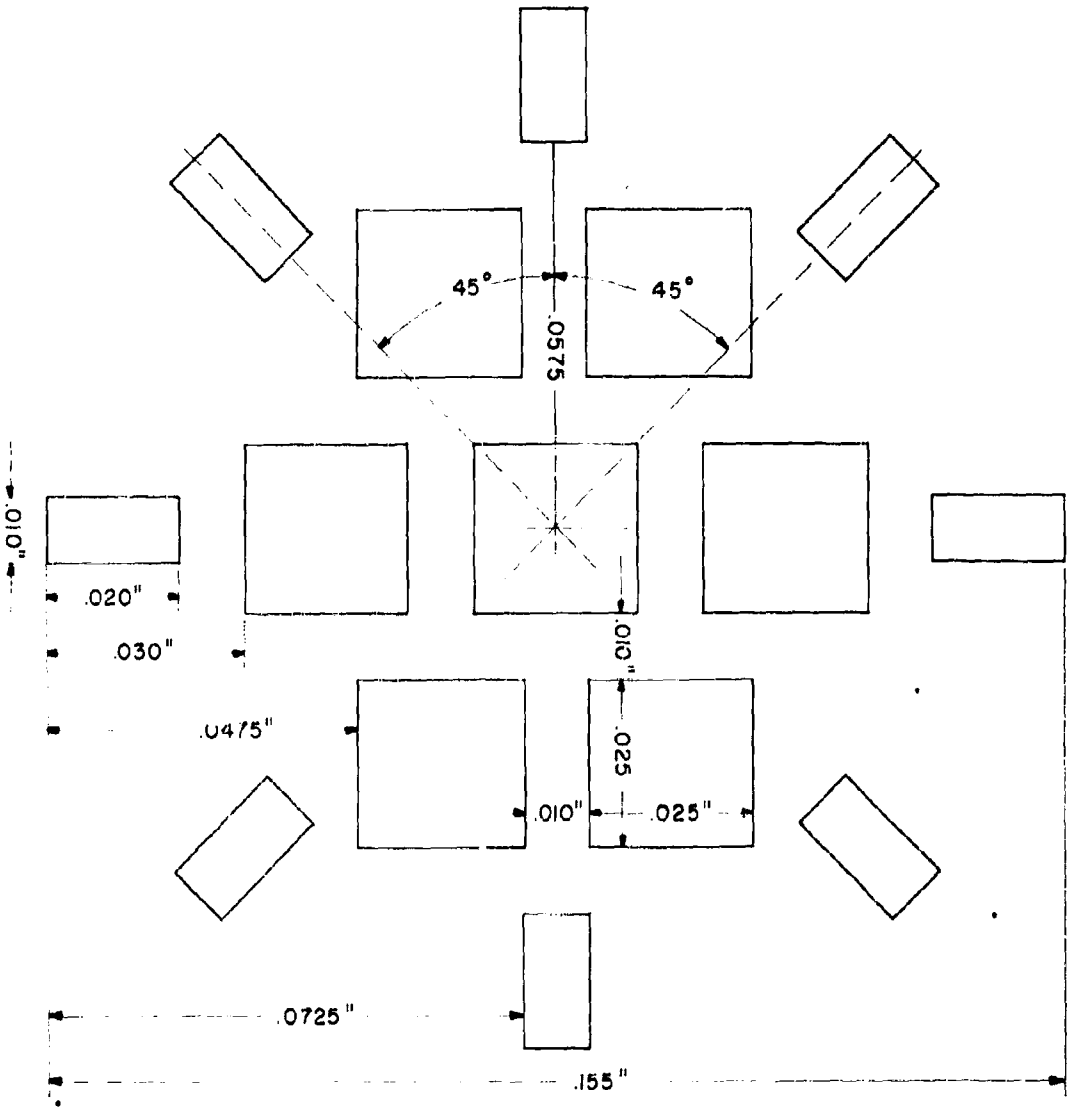


Figure 7-1. Selective Metallization Pattern for Beryllium Ceramic Disk

8.0 CIRCUIT CONSIDERATIONS

Great care is needed in selecting the circuit functions through which to demonstrate the compatibility of Integrated Circuit functions. It is the objective in Circuit and Equipment Considerations to select circuits for fabrication that satisfy the following requirements: (1) Perform a useful circuit function; (2) Be sufficiently complex to require the compatibility of a variety of processing techniques; (3) Be capable of being driven by a practical circuit; (4) Be capable of driving, or supplying signal to operate a practical circuit or function; (5) Be superior enough in some desired respect to justify the use of Integrated Circuitry.

In addition, selected circuits should satisfy the following as far as possible: (1) Be capable of realization by more than one set of Integrated Circuit Techniques; and (2) Be useful in a number of different equipment applications.

One of the first circuits selected for conversion to Integrated Circuit form was a three input NAND Logic Function. This is a digital logic circuit of a type known to be useful in many applications. All desired logical functions can be performed by various interconnections of this single design NAND. Such a logic circuit has the advantage that it can be

tested and evaluated for compatibility with associated circuitry by interconnecting a string of similar NANDS.

A schematic diagram of the NAND circuit using conventional components is shown in figure 8-1. There are a number of design features worthy of note. Since this circuit will normally be driven by one or more identical circuits and will normally drive additional identical circuits, the function of the transistor load resistor is combined with the function of the logic supply resistor. This means that the collector current for the circuit shown flows from the logic resistor and associated logic diode of the following module. If all inputs to the NAND circuit are cut off (i.e. non-conducting), the current from the combined load and logic resistor flows through the charge storage diode and across the base-emitter junction of the transistor to ground. There is always current flowing through the logic supply resistor and the drop across it is almost constant. The circuit is turned on by cutting off the previous stage or stages which drew current through one or more of the logic diodes. As current through the logic diodes diminishes, the voltage at the lower end of the logic supply resistor increases until it is sufficient to drive current through the series combination of charge storage

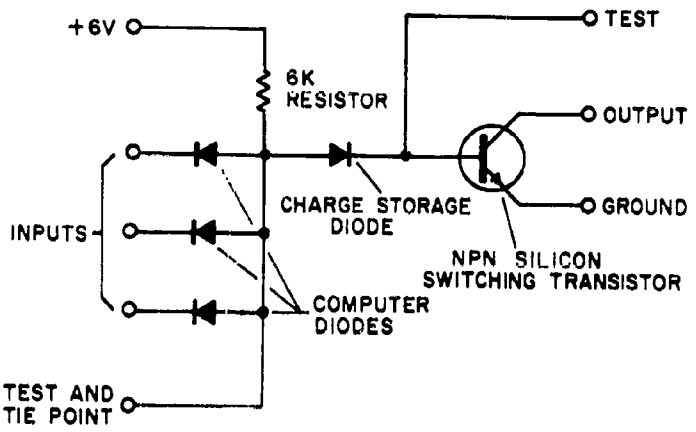


Figure 8-1. NAND Circuit

diode and transistor base-emitter junction. When sufficient current is diverted from this previous stage or stages to the present stage, the latter is turned on (and thus pulls collector current from the following stage).

The charge storage diode serves two purposes. Its knee of forward conduction, when combined with the forward voltage drop across the base-emitter junction of the transistor, forms a voltage threshold below which the transistor remains cut off. Above the threshold, the incremental resistance of the two series connected forward biased junctions drops rapidly so that in turning the circuit from off to on or vice versa, the voltage differential at the bottom of the Logic Supply Resistor is small. The second purpose of the charge storage diode is to aid in turning off the stage by removing charge carriers from the active region of the transistor. The stage is turned on by cutting off current flow through previous stages. The attendant rise in diode anode voltage is small as the circuit is turned on and similarly, during turn-off, the voltage available to sweep unwanted charge carriers from the base region of the transistor is also small. Fortunately, the circuit impedance is also small and the charge stored in

the storage diode is able to neutralize that stored in the transistor, resulting in a faster, cleaner turn-off.

In this first Integrated Circuit, all internal circuit elements are directly accessible from outside the package. Ultimately, the transistor base lead will not be brought out. The diode anode and the test point will be retained to permit multiple connection of modules for the rare cases in which more than three inputs are needed.

All the semiconductor material is silicon. The logic input diodes are fast computer diodes, the base feed diode can be slow. It must store a charge at least equal to that in the base of the transistor.

The diode-feed resistor can be made in at least three different ways:

1. As a deposited thin film upon an unmetallized portion of the alumina disc, or upon an insulated portion of the multi-diode chip.
2. As a bulk region of the multi-diode chip.
3. As a diffused biased field-effect resistor in the surface of the multi-diode chip, or a thin epitaxial back-biased layer grown on the surface.

A three stage discrete component version of this NAND (or "AND-NOT") circuit has been operated successfully at speeds of 1.mc/s with per-stage delays of 20 to 50 nanoseconds. The circuit can stand ±50% variation in supply voltage with only moderate increase in delay time. It has accepted fan-in and fan-out combinations of: 1-1, 1-3, 3-1, 3-3.

Initially, this circuit can be fabricated on three chips to permit more straightforward formation of fast and slow diodes. In this case, only the logic diodes are in the integrated form. A more challenging possibility is to fabricate it on a single chip of high resistivity material using reverse junctions for isolation and diffusing (or growing) even the collector region.

In the design of this circuit an attempt has been made to operate at the lowest practical circuit current. Operating currents of digital computer logic elements have been decreasing over the last few years in the interest of lower power drain. The advent of solid-encapsulation or Surface Passivation has helped in the task of maintaining reasonably high beta at low currents and the present embodiment is designed for 1Ma through the collector junction in the "on" condition.

The next Integrated Circuit design will be a general purpose high frequency amplifier. Conventional transistors have been made to amplify in the Darlington connection as high as 30mc, and the technique of emitter tuning presents the possibility of extending such multi-transistor action to yet higher frequencies. The multipled-collector Darlington connection and its variations have considerable charm in the eyes of Integrated Circuit designers since a common slab of semiconductor can be used as collector. Where collectors must be isolated from each other by more than a few hundred ohms of practical body resistance, back biased junctions and regions of intrinsic material will be used. The two latter cases should be capable of providing approximately 5K ohms between collectors.

A generic amplifier to fulfill the need for a universal multi-purpose device has been designed and breadboarded. It utilizes balanced transistor circuitry and has a response from dc to 0.5 mc.

An investigation of frequency selection methods was conducted to determine alternatives to the use of thin-film inductors in tuned circuits. The most promising approach

utilizes polycrystalline piezoelectric ceramic materials as resonant circuits. Circuits are being breadboarded and integrated circuits specified and designed.

9.0 INTEGRATED CIRCUIT TECHNOLOGY

There are often two fabrication steps in the development of integrated circuits:

(a) The separate pellet approach, in which the semiconductor active elements are each on separate pellets and the interconnections between active elements are all formed by fine wires bonded from element to element.

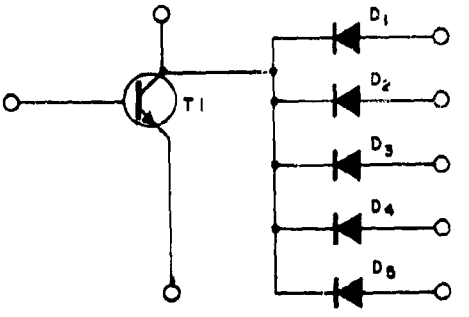
(b) The single slab approach, in which all semiconductor active elements are on a single slab of semiconductor material with a combination of (1) interconnection between active elements formed by metallized areas on the single slab, (2) interconnections within the body of the semiconductor, and (3) interconnections between active elements formed by fine wires bonded from element to element.

The separate pellet approach is necessary as an experimental step in determining the best way in which a circuit or system shall be subdivided into integrated circuit components. When operating groupings of devices are found that permit fabrication into an integrated structure, they can be built

that way. Extensive testing and redesign of the integrated circuit will generally still be necessary to "tame" the parasitics that occur when going from the separate pellet to the integrated circuit approach. Also, the process capabilities available will determine the feasibility of making a particular integrated structure.

Circuits have been fabricated using both separate pellet and integrated circuit approaches. Figure 9-1 is a photograph showing an interconnection from diode to diode by a thin aluminum film. An insulating layer of SiO_2 covers the slab except for the .002" x .006" holes through which the aluminum to silicon alloy has been formed. This SiO_2 layer acts as a mask during the diffusion processes, as well as protection for the junction. There was good adherance between the thin aluminum film and the SiO_2 layer. The main purpose of these structures, many of which were made, was to develop the technology for producing metal film conducting contacts between exposed silicon areas. The metal films must make ohmic contact to the silicon, adhere to the silicon and silicon dioxide, maintain its geometry upon alloying to the Si and SiO_2, and still leave an insulating SiO_2 layer in areas etched away after alloying. These studies have yielded metallizing

Figure 9-1. Interconnection by Thin Aluminum Film



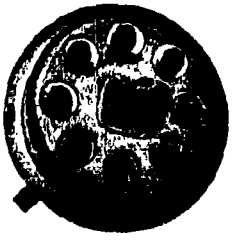


Figure 9-2. Integrated NOR Circuit on Single Silicon Slab

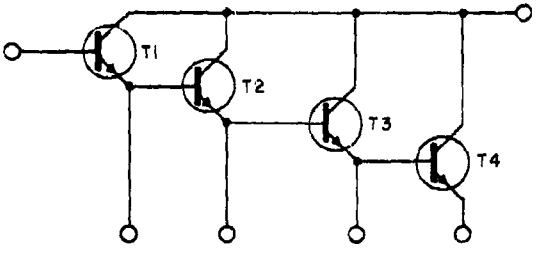


Figure 9-3. Multiple Transistor Darlington Amplifier Structure

processes that meet all the above requirements, and hence can be applied to integrated circuits in general. Further work is necessary in order to work with thinner oxide layers (<5000A) and finer metal geometries. An interesting, and perhaps useful, observation was that if aluminum is used as the metallizing agent, and alloying takes place at too high a temperature, the Al reduces the SiO_2 to form an Al-Si alloy. This can't be seen on the surface, but has a sheet resistivity low enough to be used for resistors.

Figure 9-2 is a circuit diagram of an integrated circuit which has been built on a single slab of silicon but with no thin metallic film interconnections. All connections are provided by thermo-compression bonding a wire from element to post. The circuits and slab consist of six active elements: 1 transistor and 5 diodes. The eight bonded wires are attached from active semiconductor element to post. The transistor is the element to which two wires are bonded and is in the lower left corner of the slab. The other structures are the diodes. The cathodes of the five diodes are common with the collector of the transistor.

Figure 9-3 is an illustration of the structure for a multiple transistor amplifier using the Darlington connection.

The planar passivated technology lends itself readily to conversion to processes. The next logical step in building integrated circuits is to include resistors and capacitors in the circuit.

10.0 SUMMARY OF PROJECT MAN HOURS EXPENDED DURING FIRST QUARTER

Area of Effort	Approximate Man Hours Expended
Thin Film Development	4,200
Circuit Analysis	1,000
Material Investigation	4,000
Technology	1,500
Total	10,700

APPENDIX A

THIN FILM RESISTOR POWER DISSIPATION

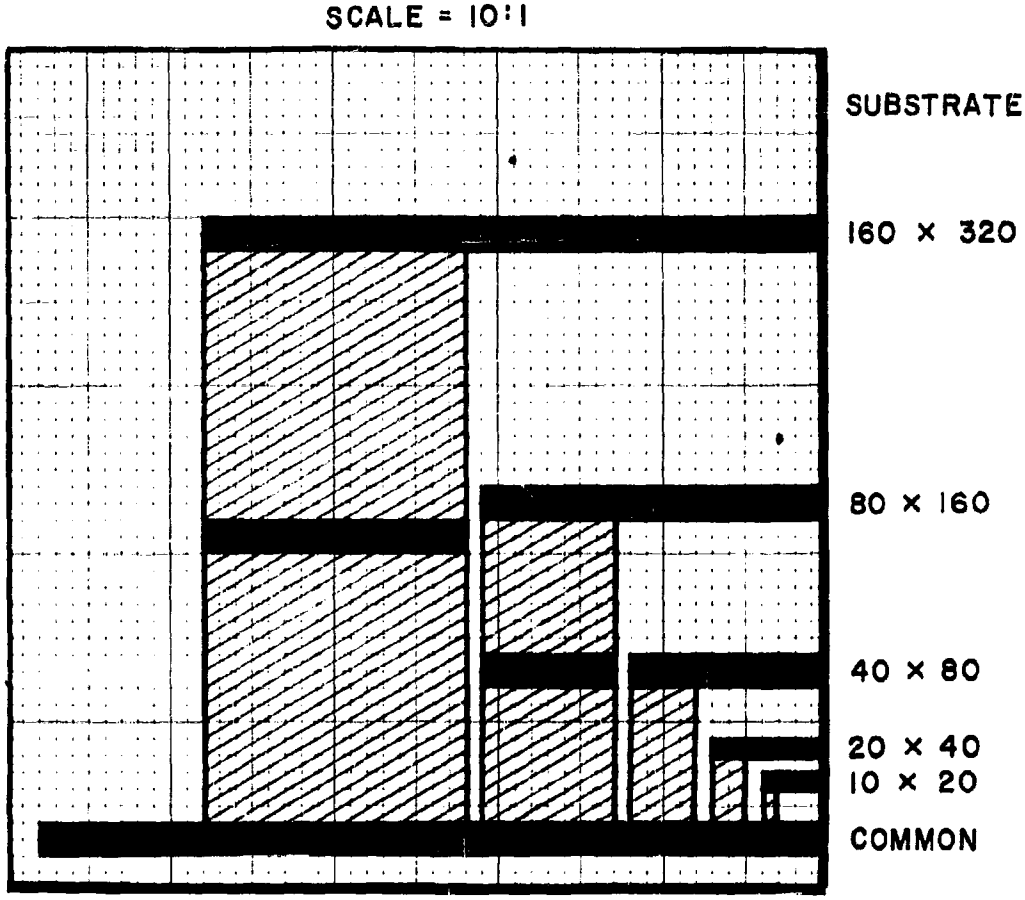
The thin-film resistors considered in this appendix are of the undoped tin oxide type.

Measurements were made under two conditions:

1. Four (4) substrates: 2 of Foto-ceram material and 2 of fused quartz were supported by terminal leads in free space. Precautions were taken to prevent air drafts from affecting results.
2. One (1) Foto-ceram substrate was attached to a small aluminum block 2 x 2 x 0.25 inches. A small amount of Dow Corning DC 4 Silicone grease was used to provide thermal conduction to the aluminum block. Heat removal from the Sink was through radiation and convection processes.

Each substrate contained 5 Undoped tin oxide resistors varying in area from 10 x 20 square mils to 160 x 320 square mils. Figure A-1 is a sketch of the substrate showing relative positions and sizes of the subject resistors.

The resistors were evaluated by applying incremental currents (2 mil ampere steps) and measuring the subsequent D.C. voltage across the resistor. Input power was increased



RESISTOR LAYOUT

Figure A-1

to a point where either the resistor was destroyed or marked change in resistance became evident.

Figure A-2 through A-6 are plots of measurements taken and are in order of increasing areas. The asterisk appearing at the end of a number of curves indicate those units which were destroyed. The circled numbers indicate the substrate material, 1 and 2 were on Fused Quartz, while numbers 3 and 4 were on Foto-ceram. Results of the tests, using the aluminum block as a heat sink, are shown in Figure A-7.

Rough estimates of power dissipation levels can be made from the curves. The table below does not take into account items such as derating factors for elevated temperature, but rather is indication of what might be considered safe bench operation levels.

AREA	DISSIPATION IN AIR(WATTS)	HEAT SINK ATTACHED(WATTS)
10 x 20	.05	0.2
20 x 40	0.10	0.4
40 x 80	0.20	1.0
80 x 160	0.30	1.5
160 x 320	0.50	2.0

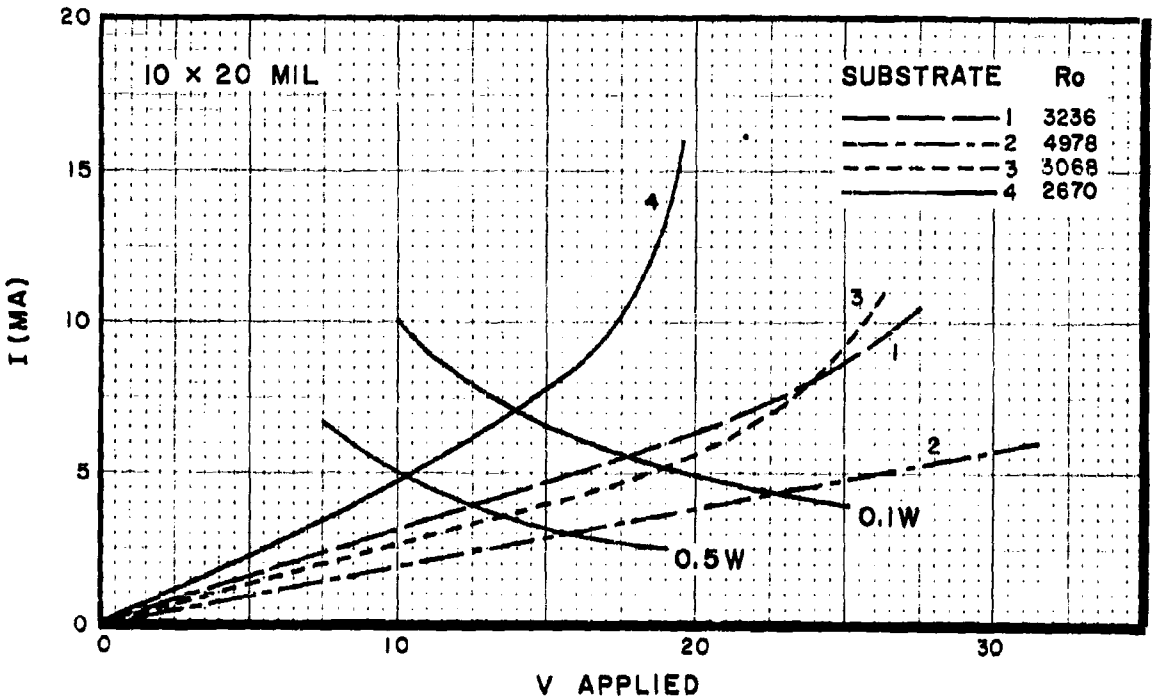

10 × 20 MIL
SUBSTRATE Ro
1 3236
2 4978
3 3068
4 2670
I (MA)
V APPLIED
0.1W
0.5W
0
5
10
15
20
30

Figure A-2

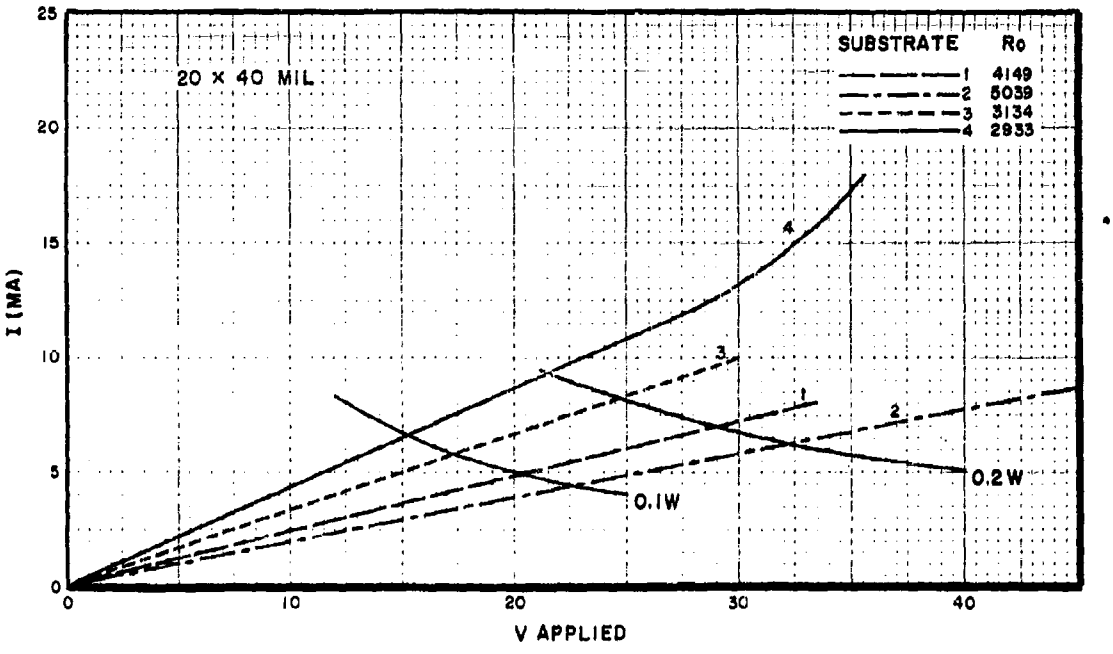

20 x 40 MIL
SUBSTRATE Ro
1 4149
2 5039
3 3134
4 2933
I (MA)
V APPLIED
0.1W
0.2W
0
5
10
15
20
25
0
10
20
30
40

Figure A-3

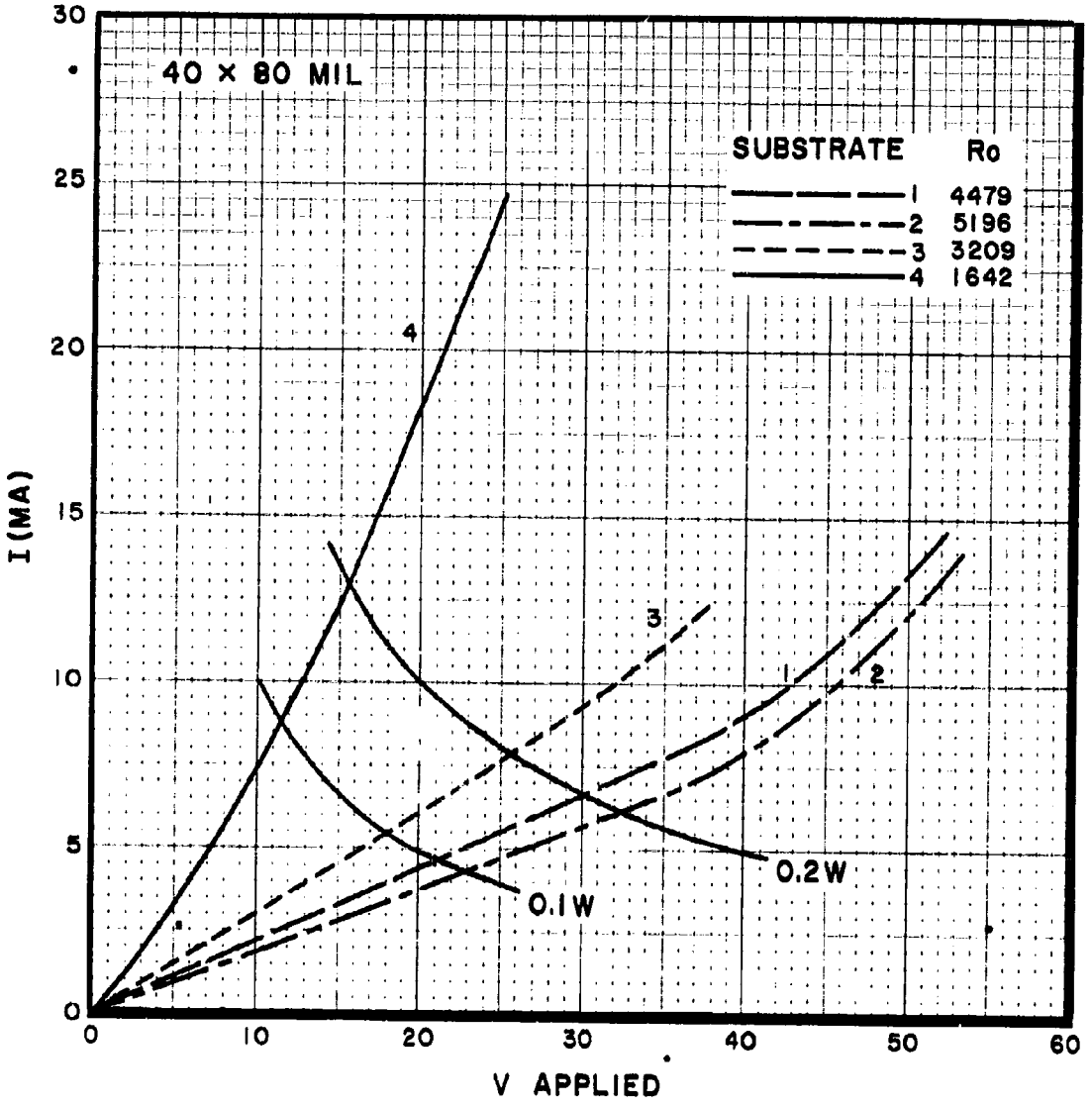

40 × 80 MIL
SUBSTRATE Ro
1 4479
2 5196
3 3209
4 1642
I (MA)
V APPLIED
0.1W
0.2W
0
5
10
15
20
25
30
0
10
20
30
40
50
60

Figure A-4

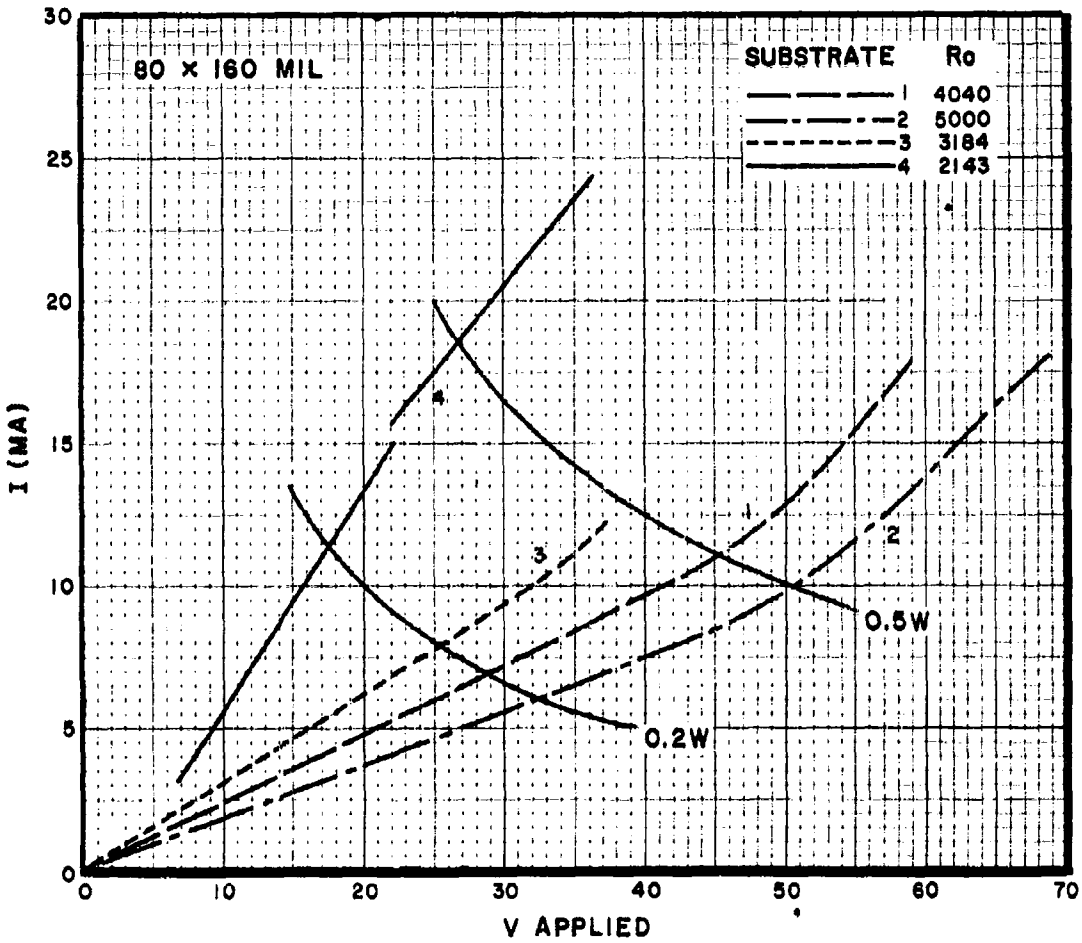

80 x 160 MIL
SUBSTRATE Ro
1 4040
2 5000
3 3184
4 2143
I (MA)
V APPLIED
0.5W
0.2W
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

Figure A-5

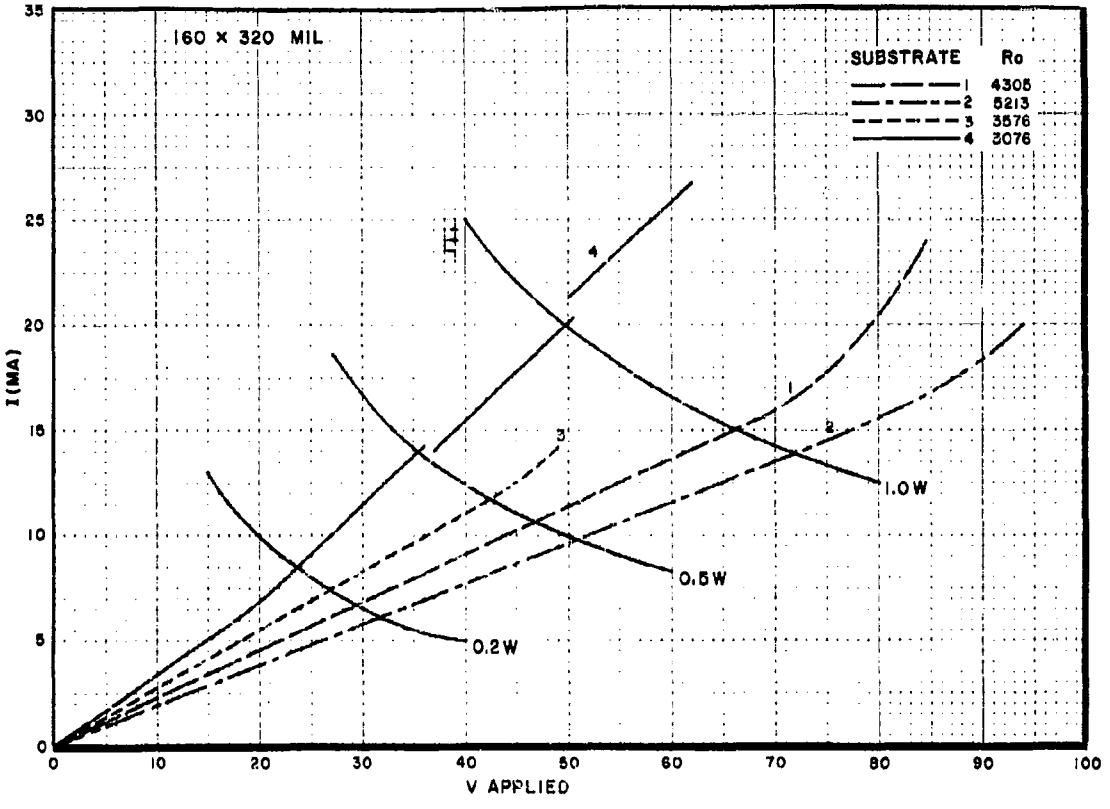

160 × 320 MIL
SUBSTRATE Rs
1 4305
2 5213
3 3576
4 3076
I(MA)
V APPLIED
1.0W
0.5W
0.2W
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
80
90
100

Figure A-6

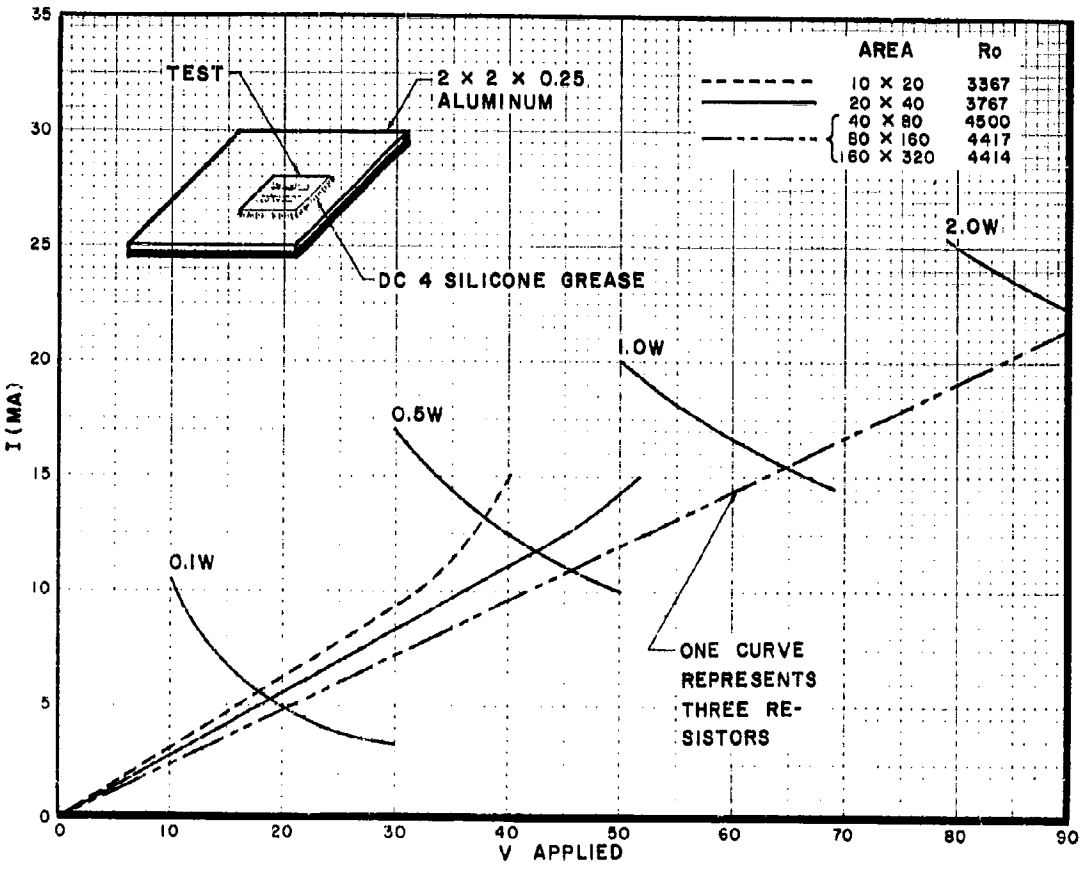

AREA
Ro
10 X 20
3367
20 X 40
3767
40 X 80
4500
80 X 160
4417
160 X 320
4414
TEST
2 X 2 X 0.25
ALUMINUM
DC 4 SILICONE GREASE
2.0W
1.0W
0.5W
0.1W
ONE CURVE
REPRESENTS
THREE RE-
SISTORS
I (MA)
V APPLIED
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
80
90

Figure A-7

APPENDIX B

PRELIMINARY REPORT ON A SURVEY OF ELECTRONIC CIRCUITRY

1.0 INTRODUCTION

1.1 A catalog of 30 generic circuit functions has been compiled by preliminary appraisal of existing circuitry. This study examines these functions to determine their validity and proposes additional functions where required.

1.2 The objective of this study is to determine the frequency of occurrence of the generic circuit functions and combinations of circuit functions.

2.0 CONCLUSIONS

2.1 The most frequent circuit function is the amplifier. The most frequent combinations are the amplifier-impedance transformer and the impedance transformer-amplifier-impedance transformer. A single circuit embodying these characteristics is an amplifier with high input resistance and low output resistance. Other circuit functions occurring frequently enough to justify attention are tabulated in Figures 3, 4, and 5. It is recommended that attention be directed only to the most frequent functions or combinations and that no significance be attached to small differences in frequency since

many variables were uncontrolled. Certain types of equipment, ECM, CECM and Telemetry, were not surveyed because the necessary schematics were not available. Therefore, some circuit functions common in these equipments do not appear in the results of this survey.

3.0 GENERIC CIRCUIT FUNCTION ANALYSIS

3.1 The list of 30 generic circuit functions was studied in order to improve it by validation or elimination of functions and by addition of new functions.

3.2 Since digital circuitry in general requires only gates, flip-flops and inverters, the digital functions have been eliminated from the list and not considered quantitatively. If digital circuitry is called for, these elements will be required in large quantities.

3.3 The function "Radiation or Absorbtion" is not generally implemented within an electronic package. The function Radiation is retained, however, to accommodate changes in the state of the art.

3.4 Functions which are not mutually exclusive, rectification and signal detection for example, are retained because no better method of describing the functions has been devised.

3.5 The function "Tuning or Control" has been classified as a modifying function. Because of its general nature, it provides little guidance in this study but is retained on the list for possible future use.

3.6 Additional functions which appeared during the survey and have been added to the list are power amplification and phase shifting. The function list as amended appears as Figure 1.

4.0 ELECTRONIC EQUIPMENT SURVEY

4.1 Because of the limited scope of the study, the equipment survey was arbitrarily confined to Motorola military electronic equipment in design, production, or recently delivered. Expansion of the survey to include a wider range of equipments could be accomplished without difficulty, although the data reduction effort would increase. The study was also limited to determining the types of functions occurring and numerical characteristics such as bandwidth or gain are omitted. Figure 2 lists the equipments studied.

4.2 The survey was implemented by examining the equipment schematics circuit by circuit and recording the circuit functions performed in the order of signal flow or data transfer.

5.0 DATA REDUCTION AND RESULTS

The frequency of occurrence of each circuit function was obtained by scanning the data and summing the individual events. The frequency of occurrence of pairs and trios of circuit functions was accomplished similarly. Tabulated results appear in Figures 3, 4, and 5.

FIGURE 1

FUNCTIONAL ELEMENT LIST

Description Number	Function
1	Frequency Generation
2	Pulse Generation
3	Voltage Amplification
4	Rectification
5	Impedance Transformation
6	Radiation
7	Attenuation
8	Frequency Modulation
9	Phase Modulation
10	Amplitude Modulation
11	Signal Detection
12	Signal Mixing
13	Pulse Counting
14	Isolation or Circulation
15	Amplitude Limiting
16	Bandwidth Limiting

FIGURE 1 (cont.)

FUNCTIONAL ELEMENT LIST

Description Number	Function
17	Analog Addition
18	Analog Multiplication
19	Deleted
20	Deleted
21	Long Time Signal Storage
22	Short Time Signal Storage
23	Tuning or Control
24	Frequency Multiplication
25	Frequency Discrimination
26	Switching or Gating
27	Signal Transmission Line
28	Electro-Mechanical Trans.
29	Electro-Optical Transducer
30	Signal Sampling
31	Power Amplification (added)
32	Phase Shifting (added)

FIGURE 2

MOTOROLA EQUIPMENTS STUDIED

1. Transponder Set, AN/APX-47 B58 A/G IFF
2. C Band Instrumentation Transponder - Bomarc
3. Panoramic Data Receiving Set, AN/URM-126
4. Field Strength Meter, AN/URM-139 (XN-1)
5. Radio Central, AN/MRC-66
6. Convair Beacon - Acquisition
7. Transponder Set, AN/DRN-11
8. PCM Coder for Bio-Satellite and Space Vehicles
9. NASA Space Receiver
10. Mark I Transponder
11. Ranger RA3 Data Encoder
12. Sarah Guidance
13. Radar Guidance Transponder, X1M-99B
14. Transponder Set, AN/APX-48 B58 A/A IFF
15. Radar Surveillance Set, AN/DPD-3
16. Transponder, SST-102A, AN/DPN-66
17. Transponder, SST-114
18. AN/APN-132 Radar, Nav.
19. Radar, Mapping, AN/APS-94

FIGURE 2 (cont.)

MOTOROLA EQUIPMENTS STUDIED

20. Radar Target Indicator AN/APS-94
21. Radar Data Receiving Set, AN/TKQ-1
22. Radar Data Transmitting Set, AN/AKT-16
23. Command Receiver, MCR-302B
24. Command Receiver, MCR-401 AN/DRW-17
25. Target Aircraft Tracking System, AN/URS-1
26. DASH
27. Airborne Transmitter, T-716/DRT

FIGURE 3

INDIVIDUAL CIRCUIT FUNCTION FREQUENCIES

Description Number	Function	Frequency of Occurrence
3	Voltage Amplification	506
5	Impedance Transformation	328
23	Tuning or Control	162
26	Switching or Gating	112
16	Bandwidth Limiting	108
15	Amplitude Limiting	87
4	Rectification	54
1	Frequency Generation	47
12	Frequency Mixing	47
31	Power Amplification	42
11	Signal Detection	37
2	Pulse Generation	33
22	Short Term Storage	32
24	Frequency Multiplication	21
10	Amplitude Modulation	14
25	Frequency Descrimination	14
29	Electro-Optical	13

FIGURE 3 (cont.)

INDIVIDUAL CIRCUIT FUNCTION FREQUENCIES

Description Number	Function	Frequency of Occurrence
27	Transmission Line	12
21	Long Term Signal Storage	9
7	Attenuation	9
13	Pulse Counting	8
17	Analog Addition Integration	7

FIGURE 4

CIRCUIT FUNCTION PAIRS

Description Numbers	Functions	Frequency of Occurrence
3 - 5	Amplifier-Impedance Transformation	156
5 - 3	Impedance Transformation-Amplifier	72
3 - 23	Amplifier-Tuning/Control	62
23 - 3	Tuning/Control - Amplifier	49
4 - 16	Rectification-Bandwidth Limiting	39
16 - 3	Bandwidth Limiting-Amplifier	35
5 - 4	Impedance Transformation-Rectification	35
3 - 15	Amplifier - Amplitude Limiting	29
3 - 26	Amplification Switching/Gating	29
3 - 16	Amplifier-Bandwidth Limiting	25
26 - 3	Switching/Gating - Amplification	25
5 - 26	Impedance Transformation - Switching	24
15 - 3	Amplitude Limiting-Amplification	23
5 - 23	Impedance Transformation - Tuning/ Control	22
3 - 31	Amplification-Power Amplification	21
11 - 3	Signal Detection - Amplification	19
16 - 15	Bandwidth Limiting - Amplitude Limiting	17

FIGURE 4 (cont.)

CIRCUIT FUNCTION PAIRS

Description Numbers	Functions	Frequency of Occurrence
23 - 5	Tuning/Control-Impedance Transformation	17
26 - 5	Switching/Gating-Impedance Transformation	16
3 - 12	Amplification - Signal Mixing	13
1 - 3	Frequency Generation-Amplification	13
12 - 3	Signal Mixing - Amplification	13
3 - 11	Amplification - Signal Detection	12
5 - 22	Impedance Transformation - Short Term Signal Storage	11

FIGURE 5

CIRCUIT FUNCTION TRIOS

Description Numbers	Function	Frequency of Occurrence
3 - 5 - 3	Amplifier-Impedance Transformation-Amplifier	24
5 - 3 - 5	Impedance Transformation - Amplifier - Impedance Transformation	15
3 - 5 - 26	Amplifier-Impedance Transformation-Switching	11
3 - 5 - 15	Amplifier-Impedance Transformation-Amplitude Limiting	11
3 - 5 - 23	Amplifier-Impedance Transformation-Control	9

APPENDIX C

THIN FILM COMPONENT VALUES REQUIRED FOR INTEGRATED CIRCUIT DESIGN

This investigation was undertaken to obtain a comparison of the range of thin film R, C, and L component values presently attainable, or soon to be attainable, with the range of component values used in common transistor circuits. Thus we can evaluate the proportion of commonly used circuits compatible with the thin film techniques as well as reveal any inadequacy in the presently planned pilot line.

To insure a random and relatively unbiased selection of circuits, all circuits (124) in NAVSHIPS 93484, "A handbook of Selected Semiconductor Circuits," were investigated. Twenty-four AC-DC and DC-DC power supply circuits were subsequently discarded as being entirely incompatible with the thin film technique because of large transformers and large values of capacitance. The 100 remaining circuits were analyzed to determine the average number of resistors and capacitors per circuit and the average number in selected ranges of resistance and capacitance per circuit. The results of this analysis are given in tabular form in Figure 1.

Resistors

Resistances of over 250KΩ will probably present problems if $S_n O_2$ of 5000 ohms/square is used. Fortunately, these large resistances are used very little except in DC and low frequency amplifiers. Resistance values of over 100KΩ are probably more of a convenience than a necessity and the lack of extremely high resistance values should not hinder circuit design.

Figure 1 demonstrates that the range of resistance covered by the 5000 ohm/square S_nO_2 film (1000Ω to 100KΩ) covers the majority of the resistance values required. This figure also reveals that in addition to the S_nO_2 resistors, each circuit will require an average of one to two resistances in the 100Ω to 1000Ω range as well as an average of one in the 0 to 100Ω range for the amplifiers. The 0 to 30Ω range can be provided by the gold chrome conducting film which has a resistance of about 3 ohms/square. The 30 ohm to 500-1000 ohm range will probably be required one to three times per circuit (substrate) and makes a resistance material in the order of 200 ohm/square necessary.

Capacitors

The capacitor data of Figure 1 indicates that, with the exceptions of switching and logic circuits, large capacitance values will present problems. Values of capacitance over 0.1 mfd to 0.2 mfd are felt to be impractical and values of over 0.02 mfd should be avoided if possible. The need for large capacitors can, in many cases, be eliminated by circuit selection and design. In many cases, capacitors may be replaced by diodes or active elements.

If 200 mmfd is assumed to represent a practical crossover value based on minimum area consideration, (from S_iO_2 to tantalum) it is probable that two Tantalum capacitors will be required for every S_iO_2 capacitor.

Inductors

The inductances listed in Figure 1 are divided into two classes; values under 10μh which may be considered feasible for present thin-film techniques, and values over 10μh which are not presently attainable. Nearly 50 per cent of the inductances used in these sample circuits are too large for thin film techniques. As is the case for capacitors, this problem may be minimized by circuit selection and design.

Conclusions

The addition of a low resistance (200 ohm/square) Nichrome evaporation station to the presently planned pilot production line will probably satisfy most design requirements.

The large value capacitance and inductance problem may be largely imaginary, i.e., these values were used in the designs studied because they were available but sizes could be greatly reduced if this reduction would result in advantages commensurate with the added complexity. It would be desirable to gain more experience in Integrated Circuit design before high L and C values are established as a priority requirement.

TYPE OF CIRCUIT	Number of Circuits of this type	Resistors Per Range Per Circuit				Average Number of resistors per ckt.	Capacitors Per Range Per Circuit					Average Number of capacitors per ckt.	Induc-tors	
		0 to 100 Ω	101 Ω to 1000 Ω	1001 Ω to 100K Ω	Over 100K Ω		Below 10 mmfd	10 mmfd to 100 mmfd	101 mmfd to .001 mfd	.0011 mfd to .01 mfd	.011 mfd to 0.1 mfd	Above 0.1 mfd		Below 10 μh	Above 10 μh
D.C. Amplifier	7	.8	1.4	5.0	1.3	8.5								0	1
Low Frequency Amplifier	16	.9	1.5	5.4	1.1	8.9	0	.3	.3	.2	.6	2.7	4.1	0	0
High Frequency Amplifier	12	.9	1.6	5.1	0	7.6	.8	1.3	1.5	1.1	2.1	1.3	8.1	16	10
Oscillators	14	0	.9	4.9	.3	6.1	.4	.6	1.3	1.0	1.2	1.5	5.9	11	13
Switching Circuits	24	.3	3.1	3.5	0	5.9	0	.7	1.0	.3	0	0	2.0	4	8
Logic Circuits	18	.1	3.1	6.5	0	9.7	0	1.4	1.0	.2	.1	.1	2.8	4	0

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